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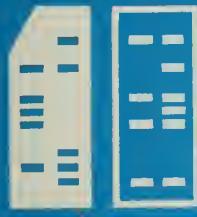
A SIMULATION STUDY OF
A DISK STORAGE ALLOCATION SYSTEM

by

Judy Ann Lender

April 30, 1970

ILLIAC IV Document No. 210



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A SIMULATION STUDY OF
A DISK STORAGE ALLOCATION SYSTEM*

by

Judy Ann Lender

April 30, 1970

Department of Computer Science
University of Illinois at Urbana-Champaign
Urbana, Illinois 61801

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ABSTRACT

This report gives a discussion of the field of simulation. The use of the simulation language SIMULA is then used to program general disk storage allocation simulators with application for use in testing allocation algorithms for the ILLIAC IV disk file allocator. Finally the concept of system design by using simulation in the design phase at various design levels is presented, with emphasis on using SIMULA for design from the hardware level upward.

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1. INTRODUCTION

There are basically three purposes for simulation: (1) studying the behavior of a system, (2) training purposes, and (3) systems design. By far, the most extensive use of simulation has been in the first two areas.

A simulator built for either or both of the first two purposes has always been built subsequent to or concurrent with the system which it is simulating. Therefore, the simulator is well-defined in the sense that the simulated system has undergone fairly extensive definition. In systems design, however, this order is reversed and a simulator is built before the design is finalized. This is a simulator of system behavior rather than a simulator of well-defined physical components, and the simulator itself is used as a tool to bring the system to a well-defined state. Of course, studying the behavior of a working system often leads to modifications in the design of that system also.

Much of this paper will describe a simulator designed for the first purpose mentioned above; that of studying the behavior of the disk file allocator algorithm for the ILLIAC IV disk. The simulator sets up a dynamic input-output environment for the disk file allocator by simulating file requests whose entries to the system are time dependent.

The objective of this paper, however, is not so much to describe and demonstrate a few lines of code, but to disclose the disciplines involved in model building and systems design. For this reason, the simulator mentioned above will be discussed only for the purpose of demonstrating the discipline of model building and simulator design. The paper will be concluded with a discussion of the use of simulation in systems design, including a short review of the literature and, finally, this author's own proposal for the use of SIMULA for this purpose.

2. MODEL BUILDING AND SIMULATION LANGUAGES

2.1 Philosophy of Model Building

Basic to every concept discussed in this paper is the notion of a "system", for it is a "system" that will be modelled and simulated. Therefore, it is necessary to define precisely what is meant by the term and related terms within the scope of this paper.

A system is a connected set of components whose behavior is self-determined. By self-determined it is meant that the state and outputs of the system can be predicted from knowledge of the previous state of the system and the inputs. A component is a device or program which is self-determined and may, in fact, be a system itself. By connected it is meant that the inputs to some of the components may be the outputs of other components of the system. A system may be a component of another system, so the distinction between system and component is one of level depending upon the system definition of the researcher doing the modelling. The most important and necessary requirement of all components defined for a particular system is that they have well-defined behavior, or it must be possible to find an algorithm which describes their behavior.

The above definitions conform to those used in the literature and, while there may be systems which do not fit the above definition, computer systems, either hardware or software, do fit the definition. It is clear that these definitions deal with the model, or static representation, of the system. The following are definitions that refer to the dynamic aspects of a simulation, or model manipulation, in order to achieve a "motion picture" of reality. The definitions will be extended later in connection with the discussions on simulation languages.

An event is an active instance of a component in time. For example, if the component happens to be a device, the event is the manipulation of that particular device as it occurs in a dynamic relationship with the other components in the system. If the component in question should be a program, the event is the execution of that program as it occurs in relation to the rest of the system. The concept of an event is one basic to any discussion of simulation and simulation languages.

This author wishes to define the term simulation in the following way, which hopefully will aid the reader in visualizing a static representation of a dynamic situation. First, however, two preliminary definitions are in order. A linear time relationship among events is one in which the events occur in increasing time intervals (simultaneity is not implied) or nondecreasing time intervals (simultaneity is implied). An event set is an ordered collection of events which exist in an increasing time relationship to one another. Finally, a simulation is a set of event sets.

Underlying the construction of any model of a real world system is a certain "way of looking at things" or discipline necessary to facilitate the description of the model. It will be seen later that simulation languages are constructed around this discipline. The remainder of this chapter is a presentation of the philosophy of model building, as applied to computers.

It should be fairly obvious by the preceding discussion that the first problem is to define the separate components of the system under investigation. These components are either fairly evident by their physical nature or are determined on the basis of their behavior relevant to the particular aspect of the system being studied.

In illustration of the criteria for determining individual components of a system, consider a dynamic storage allocation system. A general problem of the allocation type can be described by four characteristics: (1) receipt of the request, (2) allocation of the request, (3) use of the allocated space, and (4) release of the space. No dynamic storage allocation problem could be described with the omission of any one of these characteristics and, therefore, they constitute the components of the model.

Construction of the model will begin with defining the precise behavior of each of these components with respect to the particular allocation system under consideration. For example, if the times of arrival of requests are random, as is generally the case, then a queue must be added to the model to hold requests until allocation can take place.

The next problem encountered after the components of the system have been defined are the interactions of these components with one another. All relevant component interactions must be defined. For example, the component which receives the request in the dynamic storage allocation problem interacts directly with the component which performs the allocation by initiating or "calling" it, and also passes data (the request) to that component.

Two individual researchers might view a particular system differently, and it should be apparent that the definitions of the components of a particular system are by no means fixed and absolute. They exist "in the mind of the beholder" so to speak. A different way of viewing the dynamic storage allocation problem might be the following. Since allocation of this type is essentially the manipulation of a free space map, or list, the components might be defined as follows on a more physical (or structural) rather than a functional (or behavioral) basis: (1) the queue, (2) the free space list, and (3) the in-use list. Descriptions of the interactions of these components with one

another would consist of algorithms changing the physical contents of one component based on the input of another, rather than a change of state, as with a more functionally-defined component.

In summary, to construct a model of any physical system, it is necessary to determine the separate components and to describe the interactions of each of these components with the other components in the system. More specifically, these components perform actions and they are data carriers for certain other components of the system.

Therefore, definition of each of the components of the system and a description of the actions and data handled by each component will constitute a description of the model to be constructed and the simulator itself. This is the rationale behind most simulation languages; that a component is described by a discrete entity usually known as a process and that a system description in terms of the specific simulation language involved also constitutes the source code of the simulation program.

2.2 Design of Simulation Languages

2.2.1 General Consideration

One definition of a simulation model is the following: the representation of a dynamic system in a form suitable for manipulation by a computer. The key word here is "dynamic" meaning a change of state as a function of time. In defining the components of the model to be simulated, it was not necessary to consider this aspect of a simulation model. However, this aspect constitutes the major problem in the design of all simulation languages.

To get an idea of the factors determining the design of a simulation language, consider a set of events in the real world. First there is an interdependence among the events. Every real world event depends on the events preceding it and, in turn, will affect those events which succeed it.

At this time the author would like to extend the definition of an event set, keeping in mind that an event is one specific instance of a process. An event set is an ordered set of events, all members not necessarily distinct from those of a separate event set, but with the property that if one event is a member of two event sets, then all succeeding events are also members of both sets. Each event of an event set is directly activated by the preceding event and, in turn, directly activates the succeeding event. This is implied by the fact that, as stated previously, the ordering is linear by increasing times.

Second, the time-ordered occurrence and interdependency of members of an event set illustrate continuity in the set of real world events.

Third, each event is unique in that it occurs once and only once in the real world.

Finally, the real world is distinctive for its simultaneity or, in terms of the definitions given so far in this paper, it gives the appearance of being a set, or system, of event sets utilizing a common time stream.

Any simulation language must be able to deal effectively with these four aspects: interdependence, continuity, uniqueness, and simultaneity. The next section will describe how SIMULA, an ALGOL-based simulation language, handles these aspects.

2.2.2 Discussion of SIMULA

Consider first the two basic problems which must be handled by any simulation language, namely, component description and the handling of the dynamic aspects of a simulation.

SIMULA describes a component of a system as a class of processes which are described programmatically by an activity declaration, but which allows for the inclusion of SIMULA sequencing statements (to be defined later). A process can be in one of four possible states, active, suspended, passive, and terminated. If a process is active, it is currently being executed in the simulation. These states will be discussed in more detail later.

Processes can be referenced individually by a pointer to an area of memory containing the data local to the process and some additional information defining its current state of execution. These pointers are called elements. In fact, if a process must be referred to after its initial activation, the reference must be through an element representing that process. Formally, an element is declared to be of type element.

Example:

```

element pat;
activity secretary (redhaired, thumbs);
           boolean redhaired; integer thumbs;
begin. . .end;
pat:=new secretary (true,10);

```

There are two distinctions to be noted here. A process is one dynamic instance of an activity declaration which includes any of the four possible states. An event is one active instance of a process and is considered to take place in one instant of simulation system time (SST) since the computer can perform only one state change at a time, and updating the SST would itself be such a change.

The dynamic aspect of the simulation is controlled by the sequencing set (SQS) which is a set of event notices for which events have been scheduled but not completed. An event notice contains a reference to the associated process (through an element) and a real number, called its time reference. The SQS is ordered according to nondecreasing time references. The event notices at the "lower end" of the SQS is called the current event notice; its associated process is the currently active one and its time reference is regarded as the current value of the simulation system time.

Event notices in the SQS are manipulated by statements called sequencing statements. One cannot write a simulator in SIMULA or any other simulation language for that matter, nor can one satisfactorily describe a system to be simulated unless one has a clear understanding of the sequencing statements and how they affect the SQS. Similar constructs are used in other simulation languages.

Before describing the sequencing statements, it is necessary to describe in further detail the four possible states:

- (1) active--the currently active process can, by sequencing statements, alter the states of processes, including its own.
- (2) suspended--a suspended process has an associated event notice and a reactivation point, the point at which control reenters the process at the time of its next active phase, namely the place where it most recently left its previously active phase. Unless a change of state is caused by another process, the next active phase of this process will start when the event notice becomes the current one.

- (3) **passive**--a passive process has a reactivation point, but no associated event notice. It will remain passive until a change of state is caused by another process. At the time of generation a process is passive, and its reactivation point is in front of the first statement of its operation rule.
- (4) **terminated**--a process becomes terminated whenever control passes through the final end of its operation rule. Such a process has no reactivation point and no event notice. The state of a terminated process cannot be altered by ordinary sequencing statements. A process will remain part of the system at least as long as it has an associated event notice.

Sequencing statements are statements operating on the SQS, thereby altering the states of processes. A sequencing statement may delete an event notice and/or schedule an event by generating an event notice. The basic sequencing statements are:

- (1) **cancel** (<element expression>), which deletes the event notice, if any, associated with the referenced process;
- (2) **terminate** (<element expression>), which in addition to deleting the event notice, also deletes the reactivation point, if any;
- (3) **scheduling statements**, which usually generate an event notice for a specified process and include it in the SQS; in addition, the statement will specify explicitly either the time reference of the event notice, or its position in the SQS.

The basic scheduling statements are special syntactic constructs as follows:

```

activator ::= activate | reactivate

simple timing clause ::= at <arithmetic expression> |
                        delay <arithmetic expression>

timing clause ::= <simple timing clause> | <simple timing clause> prior
                    <scheduling clause> ::= <empty> | <timing clause> | before <element
                                         expression> | after <element expression>

<scheduling statement> ::= <activator> <element expression>
                           <scheduling clause>

```

The activator activate will cause the generation of an event notice only if the referenced process is passive, whereas reactivate in addition will delete the event notice associated with an active or suspended process and "reschedule" the event. A timing clause specifies the time reference of the generated event notice and this determines its position in the SQS. The event notice is normally placed behind all others with the same time reference, but it can also be placed in front of these event notices by adding the symbol prior.

The reader is referred to the paper by Dahl and Nygaard [1] and the manual on the B5500 implementation of SIMULA [2] for a more complete description of the language.

Now, consider the four characteristics of a real world system. The SIMULA construct which handles each one will now be discussed.

First, there is the characteristic of interdependence. It was mentioned earlier that a process has two aspects; it is a data carrier and it performs actions. SIMULA has a construct called a connective statement which allows a process to access the local variables of another process. Therefore, not only can one process "schedule" another process or otherwise change its event notice in the SQS, but a process can also pass parameters to another process as one would with Algol procedures, or access the local variables of another process through the connective statement.

The SQS, if all of its contents could somehow be saved throughout the simulation, would clearly be a set of event sets as defined in the preceding section. This implies that it is ordered by nondecreasing simulation system times. Continuity is maintained in that processes are activated and become current in the order of nondecreasing SSTs in the SQS.

The uniqueness of an event is inherent in its SIMULA definition, an active instance of a process which occurs once and only once throughout the simulation.

Two or more event notices can exist in the SQS with the same time reference and, even though the processes referenced by these event notices are executed by their positions in the SQS, as far as the simulation is concerned, they occur simultaneously.

3. USE OF SIMULATION FOR STUDYING CERTAIN ASPECTS OF A SYSTEM

3.1 Discussion

By far the most extensive use of simulation is in the area of studying the behavior of certain aspects of a fairly well-defined system. This implies that many hours were spent in design in conferences and at the drawing boards, and also in the fabrication of the actual system before consideration was given to a simulation study.

In constructing a simulator for this purpose, the component being studied should exist as a procedure, identical in every way to the real world component of the system; those components which directly interface with the component or constitute the input to the component under study may be required also to be procedures, or at least contain parts of the actual code of the real system. This constitutes the most important and most difficult part of simulator design, that of determining realistic driving for the component and relevant input based on the researcher's own specific purpose for the study.

If unnecessary or infeasible to give a real world definition to the components interfacing with the component under study, it is usual to design an activity giving a statistical representation of the behavior of that component. For this reason, most simulation languages include several procedures which generate random numbers according to various distributions.

3.2 The ILLIAC IV Disk File Allocator Simulator

3.2.1 The Component to be Studied--The Disk File Allocator Procedure

According to Mills and Alsberg, [4], allocation of the ILLIAC IV disk among jobs requesting space is a non-trivial programming task due to phase and channel relationships which can be specified by the programmer.

ILLIAC IV programs will be heavily I/O bound and disk latency must be minimized. Therefore, it is essential that some means be devised by which allocation algorithms can be easily tested and revised. Such a means is obviously a simulator. In the following paragraphs a simulator will be constructed according to the criteria established in earlier sections.

The Disk File Allocator takes a specific request for disk space and attempts to allocate this space by utilizing a map of free disk space. It is a modular component of the ILLIAC IV Operating System. Thus, the allocator itself exists in the simulator as a procedure, PROCEDURE ALLOCATE, in the actual coded form that it has in the operating system. It should be obvious at this point that if the real world system has a modular design, definition of some of the phases of simulating that system will be quite trivial. Another system, whose component boundaries are not well-defined might prove to be a little more difficult, and would require extra care and definition on the part of the researcher in order that no relevant factors be left out.

The allocator takes its request data from two arrays that are designed on the concept of levels of blocks. This structure of the request data is called the allocation tree. Allocation begins with the highest level in the disk hardware hierarchy, the electronic units (EUs), allocates them, and then descends through the rest of the hardware levels, the storage units (SUs), tracks (TRKs), and segments (SEGs). The blocks are arranged corresponding to this same hierarchy with an EU level block containing the EU number, the physical or virtual bit, pointers to the SU level block, the TRK level block, and the assignment block which contains specific information as to how the space is to be allocated within segments, and an indication as to whether the request is phased or contiguous or, if neither, that it is in the "junk" category, meaning that it can be allocated anywhere there are segments available.

The allocation tree, which constitutes the direct input to the allocator itself, is created by a procedure called TREEBUILD. This procedure, at the time of the design of the simulator, had been coded and debugged. A quick analysis showed the desirability of including the TREEBUILD procedure in the simulator rather than to hard code data for the allocator in the form in which it is utilized. An allocation tree is not built for a particular request until the time for an allocation attempt.

The input to TREEBUILD is in the form of a structure called a disk file block. This block is created by the job parser from ICL file specification statements at the time the request enters the operating system. As soon as the job parser is debugged, it should be added to the simulator. This will allow complete flexibility of the input in that the disk file requests may be input as ICL statements. The simulator has been designed in order to facilitate additions such as the above. Instructions for the addition are given in a later section of this report.

3.2.2 The Structure of the Simulator

3.2.2.1 Basic Structure of a Dynamic Storage Allocator System

The "core" of the simulator has been determined; it is made up of the procedures ALLOCATE and TREEBUILD, whose actual code was lifted straight from the operating system. Next, there is the problem of defining the structure of the simulator, which is primarily devoted to driving the input to procedure TREEBUILD. The output of the simulator is left entirely to the discretion of the designer and is not a factor in a discussion of the simulator structure.

Consider a general dynamic storage allocation problem, including a storage medium with a finite number of units available for allocation and a queue of requests, each for some integer less than or equal to the total number of units available for allocation, representing the number of contiguous

units of storage requested. Following allocation, these units will be held for a finite length of time and then again be made available for allocation.

As indicated in an earlier chapter, there are four main characteristics of any allocation problem: (1) receipt of the request, (2) allocation of the request, (3) the holding of the allocated space, and (4) release of the space. Since there is no constraint upon the times of arrival of requests to the system under consideration and since allocation handles only one request at a time and requires a finite amount of time for each one, a fifth characteristic, queueing of the requests, is added to this system. In the following paragraphs, each of these characteristics will be described as functional activities in the simulator, and the data they carry and the actions they perform will be discussed.

Receipt of the request. In the real world, requests enter the system at random times. Therefore, the times of entrance are chosen randomly from a uniform distribution provided by a SIMULA procedure. Actually this characteristic is best handled in the simulator by two activities, one to generate the request and the other to receive and queue it. The main difference in concept between these two procedures is that one, the activity to receive and queue the request, is part of the system and the other, the request generator, is not. This request generator is the driver of the whole simulation. If there is a system which exists entirely in the form of real-world procedures, and if its input is in the form of a driver activity, then it is still a simulator. This fact and considerations leading to it will form the basis of a subsequent chapter.

Allocation of the Request. Functionally an allocation attempt involves the following steps. First, the queue is accessed and the information on the head element of the queue is obtained. The allocator procedure then is called and an allocation attempt occurs. If the allocation was successful,

the reference to the request is removed from the queue. The request just allocated goes into the state of utilization of the allocated space, i.e., the space is unavailable for allocation to another request and it does not exist in the free space list. Obviously, if the queue is empty, then the allocation attempt is bypassed.

The above describes two separate events, the accessing of the queue and the allocation attempt. These events could have been described as two separate activities; however, they occur during the same system time in this example. If it had been desired to increment the system time by any amount between the execution of any two separate entities within the same activity, all that is needed in SIMULA is to insert reactivate current delay <increment> prior. As mentioned previously, the symbol prior places the time reference of this generated event notice in front of all others with the same time reference in the SQS.

Holding of the Allocated Space. The behavior of this phase merely constitutes a hold through several system times and simulates the behavior of some occurrence that utilizes the allocated space. The amount of time that the space is held is, of course, generated randomly, either from a uniformly distributed stream, or from some other distribution based upon previous analysis.

Release of the Allocated Space. Since simulation of the utilization of the space is only a hold, this aspect and the calling of the procedure to release the space are combined into one activity. The hold is randomly generated as mentioned above.

As a preliminary demonstration of the use of SIMULA to construct a dynamic storage allocation simulator, an algorithm for reserving variable-sized blocks of memory from a larger storage area was used. This algorithm,

and its companion algorithm for releasing this storage area, is very similar to the first-fit and liberation algorithms of Knuth [3], except that the algorithms were modified to manipulate a separate directory of available space instead of using the available space itself to contain such a list, as done in Knuth's example. This was done because the disk file allocator of the ILLIAC IV Operating System will use a free space map and because, in dealing with allocation of disk space, the nonuniform access time makes it better to maintain a separate directory of available space. The SIMULA source code and a sample of the output are given in Appendix C.

3.2.2.2 Evolution to the ILLIAC IV Disk File Allocator Simulator

No activities were added or deleted in the transition from the small simulation of Knuth's algorithms to a simulator of the ILLIAC IV allocation process. The basic ingredients of any dynamic storage allocation scheme are no different in this case. What has changed is the behavior of some of the individual activities. These will now be discussed.

The "driver" or request generator. As work progresses in this phase of the operating system, this activity often will be changed to accept input in various ways. At the present time, the activity calls a procedure which reads cards in the format of the disk file block (created by the job parser in the actual operating system) and puts the data from these cards into a file called PASSFILE which is accessed by procedure TREEBUILD. This activity contains a loop which increments a request count and then activates the process which queues the request. The request is identified in the system by its number.

One might argue that it would be more proper for the number assignment to take place within the activity which queues the request in that it is within the system and number assignment will, of course, take place within the system. By definition the driver activity does not do any more than drive the

system. It should perform none of the activities of the system. However, in a simulation designed for study of a certain aspect of a system, the aspect itself becomes the system (from the simulator's standpoint) and its boundaries are determined completely by the most convenient interpretation for the designer.

Later versions of this activity, as mentioned in an earlier section, might include the portion of the job parser which builds the disk file block from the ICL file request statements. This would provide the most flexible input. However, short of having the job parser, a suggestion for a method of input would be to set up ten or twenty data sets each representing a file block entry for one job's file requests, put these data sets into a file, and then draw randomly from this file as the simulation proceeds. Because of the simplicity of this activity, the user of the simulator may be as creative as he wishes as far as input to the system is concerned.

Activity QueueRequest. The ILLIAC IV Operating System will have several queues, called categories, each based upon a value representing maximum time requirements for execution. This value is called a timeshard and the basic timeshard unit is a quadrant minute [4].

The simulator was designed so that the researcher may read in on cards the number of queues and the value of the timeshard of each. Activity QueueRequest puts the request in the proper queue based on the execution time estimate entered with the job.

The researcher may wish to add a priority scheme within queues as such a scheme becomes defined for ILLIAC IV.

Activity Supervisor. This activity has been modified from the simple basic example more than any other, due to the ILLIAC IV Operating System's procedure for choosing the next job to be allocated. This procedure

is as follows: The supervisor goes first to the category of queue with the smallest timeshard and checks the timeslice value of the queue. If this value is greater than zero and the queue is not empty, the supervisor tries to allocate the next job in the queue, etc. If the allocation attempts for all jobs in a particular queue are unsuccessful, or if the queue is empty, or if the timeslice for the queue is less than or equal to zero, then the supervisor moves to the next queue in the order of the increasing timeshard value. If all the timeslice values of the nonempty queues are less than or equal to zero, then the timeshard value for that queue is added to the current timeslice value. If the resulting value is greater than zero, then the timeslice value is set equal to the timeshard value. This reinitializes all queues to positive timeslices.

When a successful allocation occurs, the job is removed from the queue.

Activity Jobrunning. This activity, which simulates execution time or the time that allocated space is unavailable for reallocation, was changed only to the extent that a peaked random number distribution, peaked about a certain value, was used instead of the uniform distribution. The derivation of this procedure for drawing from a peaked number distribution is given in Appendix B.1.

It should be obvious that any level of sophistication may be reached within an activity. This, again, is an illustration of the top-down approach in the study of systems. The SIMULA source code and examples of execution output are given in Appendix D.

3.2.2.3 Discussion of the Problems Encountered in Coding the Simulator

The current SIMULA translator cannot handle ALGOL constructs such as parameterized defines and case statements, both of which are used extensively in the disk file allocator and its array defines. Therefore, the source code for the simulator exists in two parts: (1) the SIMULA untranslatable portion, consisting of the disk file allocator, its procedures TREE-BUILD and ALLOCATE, and its array declarations and defines, and (2) the SIMULA translatable portion, consisting of the main SIMULA block and a few variables global to this block. This portion includes dummy declarations for those items in the untranslatable code which need to be declared to the SIMULA translator and a control section for a program called SIMULA/MERGE, which is used to merge the translated portion with the untranslatable portion prior to the ALGOL compile of the complete simulator. The translation and compilation phases of the simulator are discussed in Appendix A, and the code for SIMULA/MERGE is contained in Appendix B.2.

4. USE OF SIMULATION IN SYSTEMS DESIGN

4.1 Review of the Literature

4.1.1 The "Top Down" Approach to Systems Design

In most problem solving situations, the emphasis is first to define the problem precisely before going about devising a method of solution. However, when one considers the design of complex systems, it is not always possible to define precisely the goal of the design process. It is possible, however, to state rather definitely what functions the system is to perform, i.e., the system definition at the design stage is oriented more toward the behavioral, rather than a physical or structural, definition.

As noted in the discussion on simulation languages one factor common to all is the existence of an entity to describe a component of the system, either functional or structural. Obviously, if one has defined the behavior of the system to be designed, a simulator may be written to simulate that behavior. Then the simulated system may be broken up into components and their interconnections, specifying the behavior of each component. Then, in turn, each of these components is broken up into subcomponents with interconnections and behavior specified, and so on, until the final design level, in which units small enough to be completely designed, are obtained.

The approach just described is known as the "top down" approach to systems design and, as demonstrated, involves starting at the "top" with a complete specification of the behavior of the system and then breaking the system into smaller and smaller components until the system is specified in terms of the basic building units.

Another advantage of designing a system by the top down discipline is that it promotes modularity of the resulting system. Modular systems are

by far the easiest to debug, easiest to modify, and are by far the most aesthetically pleasing to the experienced and inexperienced system designer alike.

4.1.2 Levels of Design and Properties of Simulation Languages for Each Level

Simulation languages used for the purpose of systems design must, according to a paper by David L. Parnas and John A. Darringer [5], have certain specifications if they are to be useful. In a later article [6], Parnas indicates that the features of the language will be different, depending upon the level of design desired, level in this instance referring to levels of functional decomposition (hardware and software being indicative of a level according to this definition) rather than referring to "levels of abstraction", or the number of times a component is decomposed into subcomponents during the design phase. The word level will have both meanings in this paper and the specific meaning in context should be obvious. If the reader is confused, he is referred to the article by Parnas and Darringer [6] in which at least two paragraphs are devoted to the two meanings of the word.

Parnas and Darringer attempted to construct a language that could be used for design by simulation. In their paper [5], they give several characteristics that such a simulation language must have. However, in the later article, Parnas points out the flaws in his original language SODAS which restricted it to a very limited class of systems, that of single level computer hardware systems. In this second paper Parnas proposes some improvements and modifications to SODAS in formulating a new language, SOCS, which will allow the design of hardware and software systems of two or more levels. He refers to this computer system class as the Operating Computer Systems, since it usually includes both hardware and the software known as the operating system for the hardware. SOCS allows the design of systems in which the decision of which components are to be hardware and which are to be software may be delayed

until very late in the design. The unit Parnas selects which allows him to postpone any decisions about hardware and software is the sequential process, which he describes as a fully ordered set of events in an operating computing system that may be performed either by hardware or by software.

Parnas' languages, SODAS (Structure Oriented Description and Simulation) and SOCS (Simulations of Operating Computer Systems) and the design levels at which they are optimally used will be discussed, followed by a look at SIMULA as a potential systems design language.

The properties of the specification-design language and translator around which SODAS was designed are as follow:

(1) Designation of inputs and outputs. If these are not distinguished, then the system is likely to be overspecified (since the designer will have to produce a component that will duplicate the behavior of the algorithm on all its variables, not simply those which will be used as inputs and outputs).

(2) Combination of independently written descriptions. It must be possible to take separately written algorithms, indicate the way that inputs of one are connected with the outputs of others, without excessive worry over conflicts in names of variables, etc.

(3) Correct handling of simultaneous events. If two of the separately described components happen to be active at the same time and interact closely, the translator must correctly simulate these simultaneous events, although it is restricted to serial execution of the individual algorithms.

(4) Components which are themselves descriptions of systems. The language structure must be recursive, i.e., any system described

in the language must be acceptable as a subsystem of a system to be described in the language.

(5) Descriptions with mixed levels of detail. The design of one component may advance faster than the design of the rest of the system. It should be possible to combine a detailed description of one component with less detailed specifications of others.

(6) Mixed structural (physical) and behavioral descriptions. A structural description of a system describes it as a set of components and their interconnections; a behavioral description is an algorithm which duplicates the behavior of the system.

(7) Broad class of systems. The language must allow the description of both synchronous and asynchronous discrete systems as well as analog or continuous systems and hybrid systems.

(8) Variety of languages for component description. It is a desirable feature of a simulation system that it permit the description and simulation of systems whose components are described in quite different languages.

The main characteristics of SODAS are as follow:

A SODAS system is a set of sub-systems, each with specified inputs and outputs, together with a "wiring diagram" description of the way that the components communicate. There may be only one or any number of subsystems and the subsystems may be described in any language which has been implemented in the system, including the SODAS language itself. The simulation algorithm that is the basis of SODAS depends only on the existence of algorithms for simulating the subsystems and not at all on the language in which the algorithms were originally described. These characteristics, as far as this writer is concerned, are the "extras" that SODAS possesses as far as a

simulation language is concerned. It has, of course, all of the characteristics of the usual simulation language.

The main difficulties encountered in any attempt to use SODAS in the design of a system of two or more hardware-software levels are now discussed along with the characteristics of the language SOCS which can handle the design of such systems.

SODAS requires explicit interconnectors between components; however, it may be the case that some processes may have an explicit intercommunication because of resource sharing through global variables, and SODAS does not allow communication through global variables. There is no facility that would allow the simulation system to determine the time of an interruption of an event due to conditions not considered at earlier stages of the design without substantial modifications to a description which was actually perfectly valid for the level at which it was written. Finally, SODAS requires that all significant interconnectors between two components be specified at the time that the functions of those components are specified and that no new interconnections show up as the design progresses. In the design of operating systems, however, it is quite normal that at certain stages in a design the sequential processes may be described as entirely independent of each other, except for certain explicit attempts at communication.

Parnas lists these features that were found in SODAS but were missing in such process-oriented languages as SIMULA.

1. Ability to have a process that consists of a set of processes, e.g., recursive structure.
2. Ability to handle difficult cases of simultaneous events.
3. Ability to handle structural descriptions of hardware.
4. The "wait until" or monitoring feature proposed for SODAS.

In conclusion, Parnas describes his new language, SOCS, as being somewhat reminiscent of SIMULA with extra constructs to provide the features just mentioned. The sub-languages and connection concept would be carried over from SODAS, with a somewhat subdued role as it would be possible, but not necessary, to leave the SOCS language to describe a process. It would be desirable of the language that a SIMULA program could be run without substantial changes, though extensive surface changes might be needed.

4.2 Use of SIMULA in Systems Design

4.2.1 Discussion

This author wishes to present a method for the design of a software operating system for an existing hardware system and to show that this can be done using SIMULA as the simulation language.

The design begins, true to previous discussions, using the top-down approach. In this case, however, the behavior of the system is specified concerning the manipulation of several structural components which are the existing fixed hardware of the system. It is proposed that these physical components exist in the simulator system as processes, each simulating the behavior of its physical counterpart in the actual computer system. Unlike the other components of the simulated system these components initially are at their final stage of decomposition and are not to be modified during the design of the system.

One reason that SIMULA could not be used for design at the hardware level is that there is no specific way to declare input and output variables of activities and, therefore, there is no ability to handle structural descriptions of hardware. However, in software considerations, all interface between activities will be handled in the same way as with the procedures through the

passing of parameters and global variables and the calling of one procedure by another.

One restriction to the use of SIMULA in systems design is that the final code of the operating system be in ALGOL, the language of the simulation language. This was not a restriction as far as SODAS was concerned, providing the necessary translators were available.

The big reason why SIMULA cannot be used for design at the hardware level is that its language structure is not recursive, i.e., any system described in the language must be acceptable as a subsystem of a system to be described in the language. SIMULA does not allow activity declarations within activities. The process decomposition is one level only in SIMULA. Therefore, design of any system using SIMULA will not proceed by component decomposition, but by a similar but less defined means. In terms of ALGOL, the design will be complete when all of the system software components exist as one or more ALGOL procedures. It was mentioned in an earlier chapter that if a system is run by a driver activity simulating the input, then it is still a simulator. It is proposed then that the design be considered complete upon the arrival at the stage when the only activity existing in the simulator is the driver activity, excluding the hardware structures.

4.2.2 Example

As an example of the use of SIMULA for designing a software system, consider the design of a Version II ILLIAC IV Operating System.

Version II programs will be executed on the B6500 in ALGOL. These programs are to govern the initiation of special "algorithms" or kernels, which are sets of instructions manipulating ILLIAC IV itself. These kernels will reside on the ILLIAC IV disk.

Version II will act in a multiprogramming capacity. Four or five jobs may be in the mix simultaneously. Whether or not Version II would be feasible depends on the question of what fraction of time the PE's are idle. Obviously, it is not feasible to invest the time and money to design and code a new operating system without knowing if the effort would produce a more efficient system in terms of percentage of PE idle time compared to the corresponding data when operating under the Version I Operating System.

However, the problem very nicely fits the design by simulation using SIMULA, as described in the preceding section. The objectives are to design the system for existing hardware and to code the final operating system in ALGOL. It is impractical to proceed any other way.

This design will be a design-study application. Initially the designers are faced with four or five very well defined hardware components, as far as their behavior goes, and a set of not-very-well defined components, even as far as behavior goes, representing the modules of the Version II Operating System. Design should proceed in three stages.

Stage I--Behavior Definition of Hardware Components

It is assumed that the behavior of the hardware components are known to a great extent. This is mandatory in that the design of the operating system will depend upon the output of each of these components with respect to various inputs. It is suggested that statistical distributions be formulated for the behavior of the various hardware components for use in the operating system design. This stage may very well be the most time consuming of the whole design since all of the decisions concerning the feasibility of the Version II Operating System are governed by the behavior of these hardware components. The designer should also determine tolerance values for his data based upon his estimation of the accuracy of the models of the hardware components.

Stage 2--Behavior Definition of Software Components

In the design of this system, behavior definition of the components is a major part of the design phase. (Note that in all previous discussion, the problem of defining the behavior of the major components of the system was glossed over and made to seem trivial. This was not meant to be implied.) However, behavior definition is different in this case in that the behavior must be defined to fit existing hardware whereas, in previous discussions, behavior definition was not restricted in this manner and extended to logic elements or to "sequential processes", the division just prior to deciding which is to be hardware and which is to be software. Using a simulator to define this behavior would promote a well integrated system as a whole and would alleviate the situation of getting well into the definition of several individual components only to find that they will not work together.

Stage 3--Refinement of the Code with Activities to Become Procedures.

Once the behavior of each component has reached an optimal definition as far as the hardware is concerned, it is a relatively simple matter to refine the code within the activity to the form in which it will exist in the final system. When all of the SIMULA constructs have been coded out of the system except for one lone driver activity, then this is the final form of the operating system.

5. SUMMARY

This study served three purposes: first, the design of a flexible simulator for examining certain aspects of the allocation of files for ILLIAC IV was discussed; second, the presentation of the philosophy of simulation and, finally, the presentation of a method of systems design.

The ILLIAC IV Disk File Allocator Simulator was constructed mainly for the purpose of providing a useful means of testing the performance of the Disk File Allocator. Another use of the simulator may be to do statistical studies on the interactions between components of the Operating System interfacing with the Disk File Allocator. Another criterion considered in the construction of the simulator was that of flexibility. Each activity and procedure can be extensively changed internally and the simulator can be recompiled fairly easily.

Inherent in the design of any simulation language is the definition of the concept of systems, and a description of the system in a simulation language constitutes the simulator itself minus only the "driver" for the simulator. It is hoped that this paper has presented the philosophies of systems and simulation and their interrelationships in such a way as to facilitate the design of any system simulator.

As systems in nearly every aspect of industry become more complex each year, the prospect of design by simulation offers intriguing possibilities.* This method of design would promote systems with built-in modularity. The top-down design approach should promote greater coordination between the modules or components of the system, resulting in a more efficient system

*The design, implementation, and analysis phases all take place concurrently.

with less errors in design once the final design stage is reached. Systems analysis and study should be taking place at every level of the design allowing finalization of many design details at a much earlier time than would be the case if simulation and a proper study of the system took place after system implementation.

APPENDIX A

INSTRUCTIONS FOR
COMPILING THE SIMULATOR

Since the present SIMULA translator cannot handle constructs such as parameterized defines and case statements, both of which are used extensively in the disk file allocator and its array defines, the source code for the simulator exists in two parts: (1) the SIMULA translatable portion, consisting of the main SIMULA block and a few variables global to this block with dummy declarations for the untranslatable code, and (2) the non-SIMULA translatable portion, consisting of the disk file allocator, its procedures TREEBUILD and ALLOCATE, and its array declarations and defines.

The compilation process of this simulator takes place in three stages: (1) translation of the translatable code, (2) the merge of non-translatable code with the output of the SIMULA translation, and (3) the ALGOL compilation of the output of the merge.

The following are detailed instructions for compiling the simulator, assuming two files on disk; the translatable code, SIMULA/TI4DISK, and the untranslatable code, SIMULA/ALLOC, the disk file allocator patch deck file.

1. The execution of SIMULA/DISK will translate the SIMULA constructs into statements which can be compiled by the ALGOL compiler. In preparing the code for translation, precede each dummy section with "%BD", signifying the beginning of the section to be deleted, and end each of these sections with "%ED". Somewhere in the code between these two controls,

insert "%CP" <name of file to be inserted >, in this case, this file is SIMULA/ALLOC. (Note Appendix D.2).

The control cards for the translation are:

```
?USER=OPSYS
?EXECUTE SIMULA/DISK
?PRIORITY=3
?CORE=15000
?FILE TCODE=SIMULA/SI4DISK
?FILE DISK=SIMULA/TI4DISK
?FILE LINE=LINE BACK UP DISK
?FILE CARD=SIMDISK
?DATA SIMDISK
$DISK LIST
                                         99999999 (in columns 73-80)
?END
```

If card input is used for the code to be translated, then the control cards are:

```
?USER=OPSYS
?EXECUTE SIMULA/DISK
?PRIORITY=3
?CORE=15000
?FILE TCODE=SIMULA/SI4DISK
?FILE LINE=LINE BACK UP DISK
?FILE CARD=SIMDISK
?DATA SIMDISK
```

[source deck]

?END

(See Appendix D.1 for a sample of the translatable code, SIMULA/TI4DISK).

2. The file specified in %CP <file name> statement is now merged into the section enclosed by %BD and %ED. This merge is accomplished by executing SIMULA/MERGE, and outputs SIMULA/MI4DISK. The control cards are:

```
?USER=OPSYS
?EXECUTE SIMULA/MERGE
?FILE CARD=SIMULA/ST4DISK
?FILE NEWDECK=SIMULA/MI4DISK
?END
```

3. Finally the merged source code file SIMULA/MI⁴DISK is merged with SIMULA/GLOBAL, which contains the SIMULA procedures called in the translated code and the ALGOL compile is done, outputting the final executable code file, SIMULA/I⁴DISK. The control cards are:

```
?USER=OPSYS
?COMPILE SIMULA/I4DISK ALGOL LIBRARY
?ALGOL STACK=1000
?ALGOL FILE TAPE=SIMULA/GLOBAL DISK SERIAL
?ALGOL FILE CARE=SIMULA/MI4DISK DISK SERIAL
?END
```

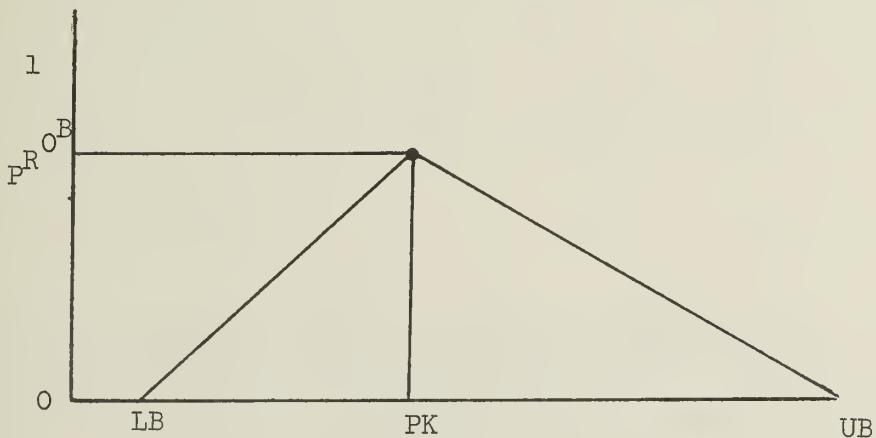
APPENDIX B

ADDITIONS TO THE B5500
IMPLEMENTATION OF SIMULA

B-1. PROCEDURE PEAKEDDRAW

This procedure allows the user to draw a number from a distribution of random numbers which is peaked about a specified number between two limits. The user specifies, as parameters to the procedure, the lower and upper limits, the value around which the numbers are peaked, and a random number drawn from a uniform distribution between 0 and 1.

The derivation of the peaked distribution was done in this way. Given a density function F peaked in the following way:



The distribution of function F is the following:

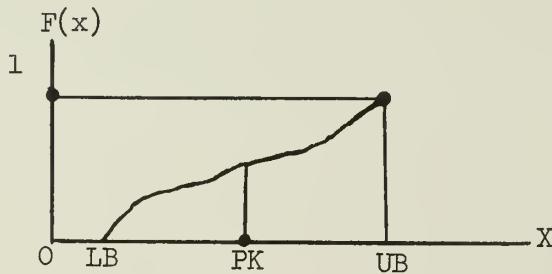
$$F(x) = \int_{-\infty}^{\infty} f(x) dx = \int_{LB}^{PK} \frac{PROB(X-LB)}{PK-LB} dx + \int_{PK}^{UB} \frac{PROB(UB-X)}{UB-PK} dx$$

Finding the value of PROB and then having an equation representing F will give us the means by which we can have a distribution function for drawing a peaked random number. We know from probability theory that

$\int_{-\infty}^{\infty} f(x) dx = 1$ and this provides a means by which the value of PROB may be

determined, given the lower bound, upper bound, and the value around which the numbers drawn are to be peaked.

Our final distribution function is then:



and the value of PK is $F^{-1}(U)$ where U is a random number drawn from a uniform number distribution between 0 and 1. After a certain amount of algebraic manipulation, the procedure is as follows:

```

REAL PROCEDURE PEAKEDDRAW (LB,UB,PEAK,UDISTR);
  VALUE LB,UB,PEAK,UDISTR; REAL LB,UB,PEAK,UDISTR;
  PEAKEDDRAW←IF UDISTRx(UB-LB)≤(PEAK-LB) THEN
    LB+SQRT(UDISTRx(PEAK-LB)x(UB-LB))
  ELSE
    UB-SQRT((UB-LB)x(UB-PEAK)x(1.0-UDISTR));
  
```

B-2. SIMULA/MERGE

The B5500 Implementation of SIMULA contains a program called SIMULA/PATCH which is supposed to allow the user to merge with ALGOL code with the translated code prior to ALGOL compilation.

However, SIMULA/PATCH does not work and the following program accomplishes the patching.

BEGIN
 COMMENT THIS PROGRAM WILL MERGE A DESIGNATED FILE WITH THE
 OUTPUT OF THE SIMULA TRANSLATOR, USING %. THIS CAN BE USED WHEN
 PROGRAMS CONTAIN PARAMETERIZED DEFINES AND CASE STATEMENTS
 WHICH THE SIMULA TRANSLATOR CANNOT HANDLE.
 FOLLOWING ARE THE COMMANDS AND WHAT THEY DO.

COMMAND	FUNCTION
%BD	REGIN DELET FILE AREA
%ED	END DELFILE AREA
%CP P/S	COPY THE FILE P/S

```

;
INTEGER INC,SEQMAX;
FILE IN CARD DISK SERIAL (2,10,30);
SAVE FILE OUT NEWDECK DISK SERIAL(20:450) (2,10,30,SAVF 99);
ARRAY A[0:9];
POINTER P1,P72;
INTEGER SEQ,LASTSEQ;
ALPHA KMND;
BOOLEAN DLTOG; %TRUE IF CARD IMAGES ARE TO BE DELETED
LABEL EOF1;
*
* DEFINE MAX(MAX1,MAX2)=
  (IF MAXA1=MAX1 GTR MAXB1=MAX2
   THEN MAXA ELSE MAXB)#
REAL MAXA,MAXB;
*
*
*
PROCEDURE COPYIT;
PBEGIN
  FILE IN DISK DISK SERIAL (2,10,30);
  POINTER PP1;
  LABEL EOF;
  INTEGER I,K;
  ARRAY PRESUF[0:3];
  I1=0;
  PP1:=P1+3;
  THRU 2 DO
    REGIN
      SCAN PP1:PP1 UNTIL IN ALPHA;
      REPLACE PTR(PRESUF[I])+1
        BY PP1:PP1 FOR K:=7 WHILE IN
          ALPHA, " " FOR K;
      IF I1=0 THEN
        PBEGIN
          SCAN PP1:PP1 UNTIL ="/";
          PP1:=PP1+1; %MOVE PAST /
          I1=2;
        END; %IF
      END; %THRU
    FILL DISK WITH PRESUF[0],PRESUF[2];
    WHILE TRUF DO
      REGIN
        READ (DISK,10,A[*])[EOF];
        REPLACE P72 BY (LASTSEQ:=LASTSEQ+INC) FOR 8 DIGITS;
        WRITE (NEWDECK,10,A[*]);
      END;
    EOF;
    END; %COPYIT
  *
```

```
%
%
P1:=POINTER(A[0]);
P72:=POINTER(A[9]);
DLTOGI:=FALSE;
IF INC LEQ 0 THEN INC:=2; %USER MAY SET INC USING COMMON
SEQMAX:=26759900-INC-1;%LAST LOC BEFORE SIMULA/GLOBAL
READ (CARD,10,A[*]);
LASTSEQ:=SEQ:=INTEGER(P72,8);
WHILE TRUE DO
  BEGIN
    COMMENT LOOK FOR COMMANDS ;
    KMND:=REAL(P1,3);
    IF KMND=="XBD" THEN DLTOGI:=TRUE ELSE
    IF KMND=="XED" THEN DLTOGI:=FALSE ELSE
    IF KMND=="XCP" THEN COPYIT
    ELSE IF NOT DLTOGI THEN
      BFGIN
        IF INTEGER(P72,8) LEQ SEQMAX THEN
          REPLACE P72 BY (LASTSEQ:=MAX(SEQ,LASTSEQ+INC))
          FOR 8 DIGITS
        ELSE LASTSEQ:=SEQ;
        WRITE (NEWDECK,10,A[*]);
      END;
      READ (CARD,10,A[*])[EOF1];
      SEQ:=INTEGER(P72,8);
    END;
  ENUF1:
  LOCK(NEWDECK);
END.
```

B-3. PROCEDURE REPLACE

The present SIMULA translator is written in ALGOL. The following procedure allows the user to replace the XALGOL construct REPLACE POINTER (A[I]) + I1 BY POINTER (B[J]) + J1 FOR K WORDS by its ALGOL equivalent.

SIMULA /REPLACE LISTED AT 9:19 ON 69298 BY OPSYS

```
STREAM PROCEDURE
REPLACE(DESTARY,DESTOFFSET,SOURCEARY,SOURCEOFFSET,COUNT);
  VALUE SOURCEOFFSET,DESTOFFSET,COUNT;
*
COMMENT REPLACE POINTER(A[I])+I1 BY POINTER(B[J])+J1 FOR K WORDS
  TRANSLATES TO:
  REPLACE (A[I],I1,B[J],J1,K);
*
BEGIN
  LOCAL DIV64,MOD64;
  DI:=LOC DIV64;SI:=LOC COUNT;SI:=SI+6;DI:=DI+7;US:=CHR;
  DI:=LOC MOD64;DJ:=DI+7;DS:=CHR;
  SI:=SOURCEARY;SI:=SI+SOURCEOFFSET;
  DI:=DESTARY;DI:=DI+DESTOFFSET;
  DIV64(US:=63 WLS;DS:=WDS);DS:=MOD64 WDS;
END REPLACE;
```

APPENDIX C

A SIMPLE DISK FILE
ALLOCATOR SIMULATOR

C-1. THE SOURCE CODE

This first section of APPENDIX C contains the source code for the simulator based on Knuth's [3] algorithms. It is assumed that there is a storage area of 20,000 units available for storage. The number of contiguous units requested is generated randomly and the allocator searches a storage directory, using the "first-fit" method, to find an available block containing an adequate number of contiguous units. When the allocated space is no longer needed, it is released as available space again.

SIMULA BEGIN

```

INTEGER M}   XQUEUE FOR REQUESTS AWAITING ALLOCATION
SET DOSSIERS  XSET OF REQUESTS SUCCESSFULLY ALLOCATED
BOOLEAN NOSPACE
BOOLEAN ALLOCATORBUSY
ELEMENT X}
ELEMENT ARRAY ALLOC[0:999]
ELEMENT ARRAY QUE[0:999]
INTEGER ARRAY WAITIME[0:999],
    RUNTIMES[0:250],
    RUNTIME[0:999]
DEFINE INDOSSIER=NUMINDOSSIER+CARDINAL(DOSSIER);
    WRITE (LN,INDOS,NUMINDOSSIER)##
DEFINE INQUEUE=NUMINQUEUE+CARDINAL(QUEUE);
    WRITE (LN,INQUE,NUMINQUEUE)##
INTEGER U;
INTEGER ALOC,ASIZES;
INTEGER NUMINQUEUEF,NUMINDOSSIERS;
INTEGER P,Q,R;
INTEGER T;
INTEGER ARRAY FREELOC[0:999],FRFESIZE[0:999],FRFELINK[0:999];
INTEGER ARRAY ALLOCNUM[0:999],ALLOCFSIZE[0:999],ALLOCLOC[0:999];
INTEGER LBDA,AVAIL;
INTEGER U1,U2,U3,U4;
REAL Z;
ALPHA QUEUEHEADS;
FILE BG 15(2,10);
FILE LN 15(2,10);
FORMAT TOP (///X35,"D I S K      M A P "///X6,"POSITION IN DIRECTORY",
    X3,"FIRST FREE UNIT",X4,"SIZE OF BLOCK",X3,
    "DIRECTORY LINK"/),
    DISKMAP (X14,X14,X17,I6,X12,I8,X10,I8);
FORMAT INDOS (//"/THE NUMBER OF REQUESTS ALREADY ALLOCATED IS ",
    I6,"."),
    INQUE ("THE NUMBER OF REQUESTS IN THE QUEUE IS ",I6,"."),
    RECREQ (//X6,"REQUEST",I5," HAS JUST COME IN FOR",I6,
    " CONTIGUOUS UNITS.","/"TIME NOW IS ",I6,"."),
    ALLOCDONE (//X6,"REQUEST",I5," WAS JUST ALLOCATED AFTER WAITING",
    I6," UNITS OF TIME",
    "IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS",
    I6," AND","/"ITS BLOCK SIZE IS",I6,
    " UNITS.","/"TIME NOW IS ",I6,"."),
    SPACENO (//X6,"WE HAVE NO SPACE ON DISK FOR REQUEST",I5,
    " IN THE QUEUE, SO WE TRY THE NEXT ELEMENT IN THE QUEUE.",
    "/"TIME NOW IS ",I6,"."),
    INTERIM (""),
    RUNDONE (//X6,"REQUEST",I5," HAS FINISHED RUNNING AFTER ",I6,
    "/"UNITS OF TIME AND ITS SPACE IS RELEASED.",
    "/"TIME NOW IS ",I6,".)
FORMAT F1 (//B1),
    F2 ("B2"),
    F3 ("B3"),
    F4 ("B4"),
    F5 ("B5"),
    F6 ("B6")##
* COMMENT PEAKEDDRAW DRAWS A RANDOM NUMBER FROM A DISTRIBUTION WHICH
IS PEAKED ABOUT A NUMBER BETWEEN A LOWER AND UPPER BOUND. 3
* REAL PROCEDURE PEAKEDDRAW (LB,UB,PEAK,UDISTR)3

```

```

VALUE LB,UB,PEAK,UDISTR; REAL LP,UB,PEAK,UDISTR;
PEAKFDDRAW+IF UDISTR*(UB-LB)≤('FAK-LB) THEN
    LB+SQRT(UDISTR*(PEAK-LB)×(UB-LB))
ELSE
    UB=SQRT((UB-LB)×(UB-PEAK)×(1.0-UDISTR)))
*
*
COMMENT PRCEDURF ALLOCATOR USES THE AVAILABLE STORAGE MAP TO
SEARCH FOR SPACE IN ACCORDANCE WITH THE NUMBER OF CONTIGUOUS BLOCKS
REQUESTED FOR A SPECIFIC REQUIST. ;
*
PROCEDURE SCHED ALLOCATOR(N);
VALUE N;
INTEGER N;
BEGIN
    LAREL A1,A2,A3,A4;
    LAREL FIN;
    INTFGR K;
COMMENT A DIRECTORY OF AVAILABLE DISK SPACE - HAS THREE ENTRIES FOR EACH
AVAILABLE BLOCK OF UNITS, FREELOC, FREESIZE, AND FREEFLINK (POINTER TO NEXT
AVAILABLE BLOCK);
A1: Q←AVAIL;
    IF FREESIZE[Q]≥N THEN
        BEGIN
            ALOC←FREELOC[Q];
            K←FREESIZE[Q]-N;
            IF K>0 THEN
                AVAIL←FREEFLINK[Q];
            ELSE
                BEGIN
                    FREELOC[Q]←FREELOC[Q]+N;
                    FREESIZE[Q]←K;
                END;
                GO TO FIN;
        END;
    END;
A2: P←FREEFLINK[Q];
    IF P=LPDA THEN
        BEGIN
            NOSPACE+TRUE;
            GO TO FIN;
        END;
A3: IF FREESIZE[P]≥N THEN
    BEGIN
        ALOC←FREELOC[P];
        K←FREESIZE[P]-N;
        IF K>0 THEN
            FREEFLINK[Q]←FREEFLINK[P];
        ELSE
            BEGIN
                FREELOC[P]←FREELOC[P]+N;
                FREESIZE[P]←K;
            END;
            GO TO FIN;
    END;
    ELSE
        BEGIN
            Q←P;
            GO TO A2;
        END;
END;
FIN:
    HOLD (RANDINT(0,10,U3));

```

```

* END ALLOCATOR;

* COMMENT PROCEDURE RELEASER RELEASES THE SPACE WHICH WAS ALLOCATED
* TO A CERTAIN REQUEST WHEN IT IS NO LONGER NEEDED.;

* PROCEDURE RELEASER (PO,N)
  VALUE PO,N
  INTEGER PO,N
  FFGIN
    LARFL B1,B2,B3,B4,B5,P6;
    NOSPACE+FALSE;
  B1: R+AVAIL;
    IF FREELOC[AVAIL]>ALLOCLOC[PO] THEN
      GO TO B5;
  B2: P+FREELINK[R];
    IF P=LRDA THEN
      GO TO B3;
    IF FREELOC[P]>ALLOCLOC[PO] THEN
      GO TO B3;
    ELSE
      FFGIN
        R+P;
        GO TO B2;
      END;
  B3: IF P!=LRDA THEN
      IF ALLOCLOC[PO]+N=FREELOC[P] THEN
        REGIN
          N+N+FREESIZE[P];
          FREELINK[PO]+FREELINK[P];
        END;
      ELSE
        FREELINK[PO]+P;
      ELSE
        FREELINK[PO]+P;
  B4: IF FFFFLOC[R]+FREESIZE[R]=ALLOCLOC[PO] THEN
      REGIN
        FREESIZE[R]+FREESIZE[R]+N;
        FRFLINK[R]+FREELINK[PO];
      END;
    ELSE
      REGIN
        FRFLINK[R]+PO;
        FREESIZE[PO]+N;
        FRFLINK[PO]+ALLOCLOC[PO];
      END;
    GO TO B6;
  B5: IF ALLOCLOC[PO]+N=FREELOC[AVAIL] THEN
      REGIN
        N+N+FREESIZE[AVAIL];
        FREELINK[PO]+FREELINK[AVAIL];
      END;
    ELSE
      FREELINK[PO]+AVAIL;
      FREELOC[PO]+ALLOCLOC[PO];
      FREESIZE[PO]+N;
      AVAIL+PO;
  B6:
    END RELEASER;

```

```

COMMENT PROCEDURE PRINTDISKMAP PRINTS THE MAP OF AVAILABLE STORAGE
SPACE, GIVING THE ADDRESS OF THE INITIAL UNIT OF A BLOCK OF FREE
SPACE AND THE NUMBER OF CONTIGUOUS UNITS IN THAT BLOCK. }

* PROCEDURE PRINTDISKMAP}
  BEGIN
    INTEGER J;
    J+AVAIL;
    WRITE (LN, TOP);
    WHILE J#LBDA DO
      BEGIN
        WRITE (LN, DISKMAP, J, FREFLOC[J], FREESIZE[J], FREELINK[J]);
        J+FREELINK[J];
      END;
    END PRINTDISKMAP;

* ACTIVITY JOBRUNNING (NUM, LOCATION, SIZE); INTEGER NUM,
  LOCATION, SIZE; FORWARD;
  ACTIVITY QUEUERFQUEST (REQFILE, RFQNUM); INTEGER REQNUM, REQFILES;
  FORWARD;

* COMMENT THE FOLLOWING ACTIVITY MAKES ALLOCATION ATTEMPTS ON EACH
  SUCCESSIVE MEMBER OF THE QUEUE UNTIL IT IS EITHER SUCCESSFUL, IN WHICH
  CASE IT ACTIVATES JOBRUNNING TO SIMULATE THE EXECUTION OF THE JOB TO
  WHICH THE SPACE WAS ALLOCATED, OR UNSUCCESSFUL IN ALLOCATING ANY
  MEMBER OF THE QUEUE, IN WHICH CASE THIS ACTIVITY TERMINATES. }

* ACTIVITY SUPERVISOR}
  BFGIN
    LABEL NEXTELEMENT;
    INTEGER J;
    IF NOT (ALLOCATORBUSY OR NOSPACE) THEN
      BEGIN
        ALLOCATORBUSY+TRUE;
        X#FIRST(QUEUE);
        IF NOT EMPTY(QUEUE) THEN
          NEXTELEMENT:
          INSPECT X WHEN QUEUERFQUEST DO
            BEGIN
              J+RFQNUM;
              ALLOCATOR (REQFILE); *MAKE AN ALLOCATION ATTEMPT
              IF NOT NOSPACE THEN
                BEGIN
                  WAITIME[REQNUM]+SIMTIME=WAITIME[REQNUM];
                  ALLOCLOC[REQNUM]+ALOC;
                  ALLOCSIZE[REQNUM]+REQFILES;
                  WRITE (LN, ALLOCONE, REQNUM, WAITIME[REQNUM],
                         ALOC, REQFILES, SIMTIME);
                END;
              REMOVE (QUE[REQNUM]);
              ALLOCATORBUSY+FALSE;
              ACTIVATE (ALLOC[REQNUM]+NEW JOBRUNNING(REQNUM,
                         ALLOCLOC[REQNUM], ALLOCSIZE[REQNUM]));
            END;
          END;
        IF NOSPACE THEN
          IF X#LAST(QUEUE) THEN
            BFGIN
              WRITE (LN, SPACENO, J, SIMTIME);
              NOSPACE+FALSE;
            END;
      END;
    END;
  END;

```

```

        X=SUC(X);
        GO TO NEXTELEMENTS;
    END;
    ALLOCATORBUSY=FALSE;
    NOSPACE=FALSE;
    FND;
END SUPERVISOR;
*
*
COMMENT ACTIVITY JOBRUNNING SIMULATES THE EXECUTION OF THE JOB TO WHICH
THE SPACE WAS ALLOCATED. THIS REPRESENTS THE TIME A CERTAIN
BLOCK IS UNAVAILABLE FOR REALLOCATION TO ANOTHER REQUEST.;

ACTIVITY JOBRUNNING (NUM,LOCATION,SIZE);
    INTEGER NUM,LOCATION,SIZE;
BEGIN
    INCLUDE (QUE[NUM],DOSSIER); % AND PUT IN DOSSIER OF RUNNING JOBS
    INDOSSIERS;
    INQUEUE;
    RUNTIMEF[NUM]←SIMTIME;
    Z←UNIFORM(0,1,U2);
    HOLD (PEAKFDDRAW(1,250,100,Z));
    RUNTIMEF[NUM]←SIMTIME-RUNTIMEF[NUM];
    T←RUNTIMEF[NUM];
    RUNTIMES[T]←RUNTIMES[T]+1;
    REMOVE (QUE[NUM]);
    RELEASESF (NUM,SIZE);
    WRITE (LN,RUNDONE,NUM,RUNTIMEF[NUM],SIMTIME);
PRINTDISKMAP;
    ACTIVATE NEW SUPERVISOR;
    FND JOBRUNNING;
*
*
COMMENT ACTIVITY QUEUEREQUEST PUTS THE NEW REQUEST INTO THE QUEUE
OF JOBS WAITING TO BE ALLOCATED AND THEN ACTIVATES THE SUPERVISOR
TO CONTROL THE ALLOCATION ATTEMPTS.;

ACTIVITY QUEUEREQUEST(REQFILES,REQNUM);
    INTEGER REQFILES;
    INTEGER REQNUM;
BEGIN
    WAITIME[REQNUM]←SIMTIME;
    INCLUDE (QUE[REQNUM],QUEUE);
    WRITE (LN,RFCREQ,REQNUM,REQFILES,SIMTIME);
    INDOSSIERS;
    INQUEUE;
    ACTIVATE NEW SUPERVISOR;
END QUEUEREQUEST;
*
*
COMMENT ACTIVITY GENERATEREQUEST GENERATES A RANDOM NUMBER BETWEEN
1 AND 2000 WHICH SIMULATES THE NUMBER OF CONTIGUOUS BLOCKS REQUESTED
BY A REQUEST. REQUESTS ARE IDENTIFIED THROUGHOUT THE PROGRAM BY
A NUMBER WHICH IS ASSIGNED TO THEM IN THIS ACTIVITY.;

ACTIVITY GENERATEREQUEST;
BEGIN
    INTEGER I;
    LABEL LOOP;
    I←1;
LOOP;

```

```
ACTIVATE (QUE[I]+NEW QUEUEREQUEST(RANDINT(1,2000,U1),T))
DELAY 0;
I←I+1;
HOLD (RANDINT(1,20,U4));
IF I≤99 THEN
  GO TO LOOP;
BARGRAPH (BG,RUNTIMES[*],40,"R");
END GENERATEREQUEST;

%
%
* M A I N      P R O G R A M
AVAIL←0;
LRDA←20000;
FREFSIZE[0]←LRDA;
FREFFL[C[0]←0;
FREFLINK[0]←LRDA;
U1←3257;
U2←46857;
U3←94823;
U4←45789;
ACTIVATE NEW GENERATEREQUEST DELAY 0;
CANCEL (CURRENT);
END SIMULA.
```

C-2. A SAMPLE OF THE EXECUTION OUTPUT

The execution output is self-explanatory. The time and the size of the block requested is noted each time a new request is generated. If a request is successfully allocated, this fact is noted on the output along with the request number, the units of simulation time that the request waited in the queue, the beginning location of the allocated space, the size of the block, and the current simulation time.

After storage is allocated and after storage is released, a free space map is printed of the available blocks of contiguous locations, indicated by the address of the first unit of the block and the size in units of the block.

When a run has been completed and the space is again released for allocation, this fact is noted on the output along with the request number, the simulated time of execution, and the current system time.

Another feature of SIMULA is the bargraph procedure in which a bar-graph of a generated distribution is printed. In this example, bargraphs were made of the waiting times in the queue (WAITIME) and the running time (RUNTIME).

REQUEST 1 HAS JUST COME IN FOR 795 CONTIGUOUS UNITS.
TIME NOW IS 0.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 0.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 1 WAS JUST ALLOCATED AFTER WAITING 6 UNITS OF TIME
IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 0, AND
ITS BLOCK SIZE IS 795 UNITS.
TIME NOW IS 6.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
0	795	19205	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 1.
THE NUMBER OF REQUESTS IN THE QUEUE IS 0.

REQUEST 2 HAS JUST COME IN FOR 1230 CONTIGUOUS UNITS.
TIME NOW IS 12.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 1.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 2 WAS JUST ALLOCATED AFTER WAITING 6 UNITS OF TIME
IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 795, AND
ITS BLOCK SIZE IS 1230 UNITS.
TIME NOW IS 18.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
0	2025	17975	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 2.
THE NUMBER OF REQUESTS IN THE QUEUE IS 0.

REQUEST 3 HAS JUST COME IN FOR 1467 CONTIGUOUS UNITS.
TIME NOW IS 22.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 2.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 3 HAS JUST ALLOCATED AFTER WAITING 5 UNITS OF TIME
IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 2025, AND
ITS BLOCK SIZE IS 1467 UNITS.
TIME NOW IS 27.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
0	3492	16508	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 3.
THE NUMBER OF REQUESTS IN THE QUEUE IS 0.

REQUEST 4 HAS JUST COME IN FOR 130 CONTIGUOUS UNITS.
TIME NOW IS 40.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 3.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 4 HAS JUST ALLOCATED AFTER WAITING 0 UNITS OF TIME
IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 3492, AND
ITS BLOCK SIZE IS 130 UNITS.
TIME NOW IS 40.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
0	3622	16378	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 4.
THE NUMBER OF REQUESTS IN THE QUEUE IS 0.

REQUEST 5 HAS JUST COME IN FOR 19 CONTIGUOUS UNITS.
TIME NOW IS 48.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 4.

THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 5 WAS JUST ALLOCATED AFTER WAITING 6 UNITS OF TIME IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 3627, AND ITS BLOCK SIZE IS 19 UNITS. TIME NOW IS 54.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
0	3641	16359	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 5.
THE NUMBER OF REQUESTS IN THE QUEUE IS 0.

REQUEST 6 HAS JUST COME IN FOR 719 CONTIGUOUS UNITS.
TIME NOW IS 60.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 5.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 7 HAS JUST COME IN FOR 1520 CONTIGUOUS UNITS.
TIME NOW IS 61.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 5.
THE NUMBER OF REQUESTS IN THE QUEUE IS 2.

REQUEST 6 WAS JUST ALLOCATED AFTER WAITING 6 UNITS OF TIME IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 3641, AND ITS BLOCK SIZE IS 719 UNITS.
TIME NOW IS 66.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
0	4360	15640	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 6.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 8 HAS JUST COME IN FOR 413 CONTIGUOUS UNITS.
TIME NOW IS 74.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 6.
THE NUMBER OF REQUESTS IN THE QUEUE IS 2.

REQUEST 7 WAS JUST ALLOCATED AFTER WAITING 18 UNITS OF TIME
IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 4360, AND
ITS BLOCK SIZE IS 1520 UNITS.
TIME NOW IS 79.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
0	5880	14120	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 7.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 9 HAS JUST COME IN FOR 1848 CONTIGUOUS UNITS.
TIME NOW IS 94.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 7.
THE NUMBER OF REQUESTS IN THE QUEUE IS 2.

REQUEST 8 WAS JUST ALLOCATED AFTER WAITING 28 UNITS OF TIME
IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 5880, AND
ITS BLOCK SIZE IS 413 UNITS.
TIME NOW IS 102.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
0	6293	13707	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 8.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 10 HAS JUST COME IN FOR 1205 CONTIGUOUS UNITS.
TIME NOW IS 107.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 8.
THE NUMBER OF REQUESTS IN THE QUEUE IS 2.

REQUEST 9 WAS JUST ALLOCATED AFTER WAITING 20 UNITS OF TIME
IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 6293, AND
ITS BLOCK SIZE IS 1848 UNITS.
TIME NOW IS 114.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
0	8141	11859	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 9.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 11 HAS JUST COME IN FOR 144 CONTIGUOUS UNITS.
TIME NOW IS 116.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 9.
THE NUMBER OF REQUESTS IN THE QUEUE IS 2.

REQUEST 10 WAS JUST ALLOCATED AFTER WAITING 17 UNITS OF TIME
IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 8141, AND
ITS BLOCK SIZE IS 1205 UNITS.
TIME NOW IS 124.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
0	9346	10654	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 10.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 4 HAS FINISHED RUNNING AFTER 89
UNITS OF TIME AND ITS SPACE IS RELEASED.
TIME NOW IS 129.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
4	3492	130	0
0	9346	10654	20000

REQUEST 3 HAS FINISHED RUNNING AFTER 102 UNITS OF TIME AND ITS SPACE IS RELEASED.
TIME NOW IS 129.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
3	2025	1597	0
0	9490	10510	20000

REQUEST 11 WAS JUST ALLOCATED AFTER WAITING 15 UNITS OF TIME IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 9346, AND ITS BLOCK SIZE IS 144 UNITS.
TIME NOW IS 131.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
3	2025	1597	0
0	9490	10510	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 0.
THE NUMBER OF REQUESTS IN THE QUEUE IS 0.

REQUEST 12 HAS JUST COME IN FOR 295 CONTIGUOUS UNITS.
TIME NOW IS 132.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 0.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 12 WAS JUST ALLOCATED AFTER WAITING 10 UNITS OF TIME IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 2025, AND ITS BLOCK SIZE IS 295 UNITS.
TIME NOW IS 142.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
82	208	543	81
81	717	413	87
87	923	835	79
79	1926	5643	48
48	10399	9601	67
67	18386	1378	20000

REQUEST 96 HAS JUST COME IN FOR 1360 CONTIGUOUS UNITS.
TIME NOW IS 1075.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 7.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 95 HAS FINISHED RUNNING AFTER 17
UNITS OF TIME AND ITS SPACE IS RELEASED.
TIME NOW IS 1079.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
82	208	543	81
81	717	413	87
87	923	835	95
95	1130	796	79
79	3286	4283	48
48	10399	9601	67
67	18386	1378	20000

REQUEST 96 WAS JUST ALLOCATED AFTER WAITING 5 UNITS OF TIME
IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 1926 AND
ITS BLOCK SIZE IS 1360 UNITS.
TIME NOW IS 1080.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
82	208	543	81
81	717	413	87
87	923	835	95
95	1130	796	79
79	3286	4283	48
48	10399	9601	67
67	18386	1378	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 7.
THE NUMBER OF REQUESTS IN THE QUEUE IS 0.

REQUEST 97 HAS JUST COME IN FOR 685 CONTIGUOUS UNITS.
TIME NOW IS 1093.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 7.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 83 HAS FINISHED RUNNING AFTER 163
UNITS OF TIME AND ITS SPACE IS RELEASED.
TIME NOW IS 1093.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
82	208	543	81
81	717	413	83
83	751	172	87
87	1608	150	95
95	1130	796	79
79	3286	4283	48
48	10399	9601	67
67	18386	1370	20000

REQUEST 97 WAS JUST ALLOCATED AFTER WAITING 1 UNITS OF TIME
IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 923, AND
ITS BLOCK SIZE IS 685 UNITS.
TIME NOW IS 1094.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
82	208	543	81
81	717	413	83
83	751	172	87
87	1608	150	95
95	1130	796	79
79	3286	4283	48
48	10399	9601	67
67	18386	1370	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 7.

THE NUMBER OF REQUESTS IN THE QUEUE IS 0.

REQUEST 98 HAS JUST COME IN FOR 1657 CONTIGUOUS UNITS.
TIME NOW IS 1112.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 7.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 92 HAS FINISHED RUNNING AFTER 78
UNITS OF TIME AND ITS SPACE IS RELEASED.
TIME NOW IS 1115.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
92	0	499	82
82	208	543	81
81	717	413	83
83	751	172	87
87	1608	150	95
95	1130	796	79
79	4943	2626	48
48	10399	9601	67
67	18386	1376	20000

REQUEST 98 WAS JUST ALLOCATED AFTER WAITING 9 UNITS OF TIME
IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 3286, AND
ITS BLOCK SIZE IS 1657 UNITS.
TIME NOW IS 1121.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
92	0	499	82
82	208	543	81
81	717	413	83
83	751	172	87
87	1608	150	95
95	1130	796	79
79	4943	2626	48
48	10399	9601	67
67	18386	1376	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 7.
THE NUMBER OF REQUESTS IN THE QUEUE IS 0.

REQUEST 99 HAS JUST COME IN FOR 1907 CONTIGUOUS UNITS.
TIME NOW IS 1126.

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 7.
THE NUMBER OF REQUESTS IN THE QUEUE IS 1.

REQUEST 99 WAS JUST ALLOCATED AFTER WAITING 4 UNITS OF TIME
IN THE QUEUE. ITS BEGINNING BLOCK LOCATION ON DISK IS 4943, AND
ITS BLOCK SIZE IS 1907 UNITS.
TIME NOW IS 1130.

D T S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
92	0	499	82
82	208	543	81
81	717	413	83
83	751	172	87
87	1608	150	95
95	1130	796	79
79	6850	719	48
48	10399	9601	67
67	18386	1376	20000

THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 8.
THE NUMBER OF REQUESTS IN THE QUEUE IS 0.

REQUEST 86 HAS FINISHED RUNNING AFTER 163
UNITS OF TIME AND ITS SPACE IS RELEASED.
TIME NOW IS 1136.

D T S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
92	0	499	82
82	208	543	81
81	717	413	83
83	751	172	87
87	1608	150	95
95	1130	796	79
79	6850	1965	48
48	10399	9601	67
67	18386	1376	20000

REQUEST 94 HAS FINISHED RUNNING AFTER 83
 UNITS OF TIME AND ITS SPACE IS RELEASED.
 TIME NOW IS 1143.

D T S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
92	0	499	94
94	0	751	81
81	717	413	83
83	751	172	87
87	1608	150	95
95	1130	796	79
79	6850	1905	48
48	10399	9601	61
67	18386	1378	20000

REQUEST 91 HAS FINISHED RUNNING AFTER 151
 UNITS OF TIME AND ITS SPACE IS RELEASED.
 TIME NOW IS 1173.

D T S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
92	0	499	94
94	0	751	81
81	717	413	83
83	751	172	87
87	1608	150	95
95	1130	796	79
79	6850	13150	61
67	18386	1378	20000

REQUEST 99 HAS FINISHED RUNNING AFTER 55
 UNITS OF TIME AND ITS SPACE IS RELEASED.
 TIME NOW IS 1185.

D T S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
92	0	499	94
94	0	751	81

81	717	413	83
83	751	172	87
87	1608	150	95
95	1130	796	99
99	4943	15057	67
67	18386	1378	20000

REQUEST 96 HAS FINISHED RUNNING AFTER 112
 UNITS OF TIME AND ITS SPACE IS RELEASED.
 TIME NOW IS 1192.

D T S F M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
92	0	499	94
94	0	751	81
81	717	413	83
83	751	172	87
87	1608	150	95
95	1130	2156	99
99	4943	15057	67
67	18386	1378	20000

REQUEST 93 HAS FINISHED RUNNING AFTER 198
 UNITS OF TIME AND ITS SPACE IS RELEASED.
 TIME NOW IS 1248.

D T S F M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
92	0	499	94
94	0	751	93
93	490	671	63
83	751	172	87
87	1608	150	95
95	1130	2156	99
99	4943	15057	67
67	18386	1378	20000

REQUEST 98 HAS FINISHED RUNNING AFTER 137
 UNITS OF TIME AND ITS SPACE IS RELEASED.
 TIME NOW IS 1258.

D T S F M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
92	0	499	94
94	0	751	93
93	499	631	83
83	751	172	87
87	1608	150	95
95	1130	18870	67
67	18386	1378	20000

REQUEST 97 HAS FINISHED RUNNING AFTER 235
 UNITS OF TIME AND ITS SPACE IS RELEASED.
 TIME NOW IS 1329.

D I S K M A P

POSITION IN DIRECTORY	FIRST FREE UNIT	SIZE OF BLOCK	DIRECTORY LINK
92	0	499	94
94	0	751	93
93	499	631	83
83	751	1007	95
95	1130	18870	67
67	18386	1378	20000

APPENDIX D

THE ILLIAC IV DISK FILE
ALLOCATOR SIMULATORD-1. THE SIMULA TRANSLATABLE PORTION -- The Simulator Skeleton
(SIMULA/TI4DISK).

The first section of Appendix D contains the SIMULA translatable portion of the simulator including the SIMULA constructs, namely, the SIMULA block containing the element and set declarations and the activity declarations.

As stated previously, the current version of the B5500 implementation of SIMULA will not accept parameterized defines or case statements; therefore, all code containing these constructs has been removed from this skeleton portion of the simulator before the SIMULA translation, but will be merged with the translated SIMULA code just prior to ALGOL compilation.

```

XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
X
X SIMULA/TI4DISK--THE TRANSLATABLE PORTION
X
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
X
X
X BEGIN
X INTEGER I;
X INTEGER QUEENUM;
X INTEGER ARRAY TMFSHARD[0:99];
X INTEGER T;
X FILE CD(2,10));
X FILE SIMFILE 15(2,15));
X FORMAT FQUEENUM (T2),
X           FSHARDNUM (I3));
X DEFINE LN=SIMFILE#
X
X COMMENT THE FOLLOWING PROCEDURE ALLOWS THE TRANSFER OF XALGOL
X REPLACE STATEMENTS INTO EQUIVALENT ALGOL STATEMENTS;
X
X STREAM PROCEDURE
X REPLACE(DESTARY,DESTOFFSET,SOURCEARY,SOURCEOFFSET,COUNT)
X VALUE SOURCEOFFSET,DESTOFFSET,COUNT;
X
X COMMENT REPLACE PTR(A[I])+I1 BY PTR(P(J1)+J1) FOR K
X TRANSLATES TO:
X REPLACE (A[I],I1,E[J],J1,K);
X
X BEGIN
X LOCAL DIV64,MOD64;
X DIV64:=LOC(F1V64);ST:=LOC(COUNT);SI:=ST+6;TI:=(I+7)DIV4;
X DI:=LOC(MOD64);DI:=DT+7;DS:=CHR();
X SI:=SOURCEARY;ST:=SI+SOURCEOFFSET;
X DI:=DESTARY;DI:=DI+DESTOFFSET;
X DIV64;DS:=63;WDS;DS:=WDS);DS:=MOD64;WES;
X END REPLACE;
X
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
X
X BEGIN SIMULA/MERGE CONTROL SECTION
X
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
X
X ED
X PROCEDURE TREBUILD; 9DUMMY PROCEDURE
X FEGIN
X FEND;
X
X PROCEDURE ALLOCATE; 9DUMMY PROCEDURE
X FEGIN
X FEND;
X CP SIMULA/ALLOC
X
X PROCEDURE READEMS; 9DUMMY PROCEDURE
X FEGIN
X FEND;
X

```

```

PROCEDURE WRITEM;  %DUMMY PROCEDURE
  BEGIN
  END;

%
%ED
%
%%%%%%%%%%%%%
%
% END SIMULA/MERGE CONTROL SECTION
%
%%%%%%%%%%%%%
%
%
READ (CD,FQUEENUM,QUEENUM);
QUEENUM:=QUEENUM-1;  %NUMBER OF QUEUES IN SYSTEM
FOR I=0 STEP 1 UNTIL QUEENUM DO
  READ (CD,FSHARDNUM,TIMESHARD[I]);
%
%
COMMENT THIS SECTION BEGINS THE SIMULA BLOCK.  ALL SIMULA CON-
STRUCTS, ELEMENTS, SETS, AND ACTIVITIES ARE DEFINED IN THIS
BLOCK.  NO PARAMETERIZED DEFINES OR CASE STATEMENTS MAY OCCUR HERE.%
%
%
%%%%%%%%%%%%%
SIMULA BEGIN
%%%%%%%%%%%%%
  INTEGER M;
  SET ARRAY QUEUF[0:QUEENUM];  %REQUEST QUEUE
  SET DOSSIER;  %SET OF REQUESTS SUCCESSFULLY ALLOCATED
  BOOLEAN NOSPACE;
  BOOLEAN ALLOCATORBUSY;
  ELEMENT X;
  ELEMENT ARRAY QUE[0:999];
  INTEGER ARRAY WAITIME[0:999],
             RUNTIME[0:999],
             TIMESLICE[0:QUEENUM],
             TREFBUILDTIME[0:999],
             ALLOCETIME[0:999];
  DEFINE NEQ=##,
        LSS=<#,
        GTR=>#,
        LEQ=<=,
        GEQ=>=;
%
% THE FIRST TWO DEFINES GIVE THE NUMBER OF ITEMS IN THE SET
% DOSSIER AND QUEUE[M]
%
  DEFINE INDOSSIER=NUMINDOSSIER+CARDINAL(DOSSIER);
          WRITE (LN,INDOS,NUMINDOSSIFR)%;
  INQUEUES=FOR M=0 STEP 1 UNTIL QUEENUM DO
    BEGIN
      NUMINQUEUE[M]=CARDINAL(QUEUE[M]);
      WRITE (LN,INQUE,M,NUMINQUEUE[M]);
    END%;
%
% THIS PRINTS THE CURRENT VALUES OF THE TIMESHARD AND TIMESLICE
% FOR A PARTICULAR QUEUE
%
  QUEUEINFO=WRITE (LN,INTERIM);
          FOR M=0 STEP 1 UNTIL QUEENUM DO

```

```

      WRITE (LN,FSLICE,M,TIMESHARD(M),TIMESLICF(M))#
INTEGER U1,U2,U3,U4,U5#
INTEGER NUMINDOSSIERS#
INTEGER ARRAY NUMINQUEUE[0:99]#
INTEGER ARRAY FREFLOC[0:999],FREESIZE[0:999],FRFLINK[0:999]#
INTEGER ARRAY ALLOCNUM[0:999],ALLOCSIZE[0:999],ALLOCLOC[0:999]#
REAL Z#
FORMAT INDOS ("SIM==THE NUMBER OF REQUESTS ALREADY ALLOCATED IS ",#
               I6,"."),
     INQUE ("SIM==THE NUMBER OF REQUESTS IN QUEUE",I2,") IS ",#
               I4,"."),
     FSLICE ("SIM==QUEUE",I2,")=",X5,"TIMESHARD IS ",I6,#
               " UNITS. TIMESLICE IS ",I6," UNITS."),
     FTB("SIM==REQUEST ",I5," = PROCESSOR TIME FOR TREEBUILD IS ",#
               I6,"."//"/"),
     FAT("SIM==REQUEST ",I5," = PROCESSOR TIME FOR ALLOCATION IS ",#
               I8,"."),
     FURMIN(///"SIM==REQUEST ",I5," HAS JUST ENTERED QUEUE ",I3,#
               " AT SIMULATION TIME ",I6,"."),
     FALLOC (///"SIM==REQUEST ",I5,#
               " WAS JUST ALLOCATED AFTER WAITING ",I5,#
               " UNITS OF SIMULATION TIME IN QUEUE ",I3/
               "SIM==SIMTIME NOW IS ",I6,"."),
     FSEARCH ("SIM==ALLOCATION ATTEMPT TO BE MADE ON QUEUE",#
               I2,"."),
     FTHRU (///"SIM==REQUEST ",I3," IS FINISHED AFTER ",#
               I5," UNITS OF TIME."),
     INTERIM (" ")
#
#
REAL PROCEDURF PEAKEDDRAW(LB,UB,PEAK,UDISTR)#
VALUE LB,UB,PEAK,UDISTR; REAL LB,UB,PEAK,UDISTR;
PEAKEDDRAW < IF UDISTR*(UB-LB) ≤ (PEAK-LB) THEN
                  LB+SQRT(UDISTR*(PEAK-LB)*(UP-LB))
                ELSE
                  UP-SQRT( (UP-LB)*(UP-PEAK)*(1.0-UDISTR) )
#
#
#
#####
# SIMULATOR ACTIVITY DECLARATIONS
#####
#
#
ACTIVITY JOBRUNNING (NUM,WHICHQ1:QUEU) INTEGER NUM,WHICHQUEUE;
FORWARD;
ACTIVITY QUEUEREQUEST (REQNUM) INTEGER REQNUM;LOCALS
  INTEGER QUENUM;FORWARD;
#
#
COMMENT THE FOLLOWING ACTIVITY CHECKS EACH QUEUE AND ON THE BASIS
OF ITS TIMESLICE VALUE, EITHER SELECTS A JOB FROM THIS QUEUE OR
CONTINUES ON TO THE NEXT QUEUE. IF THERE IS AN ALLOCATION
ATTEMPT ON A REQUEST WITHIN A QUEUE AND IT FAILS, THE NEXT
REQUEST IN THE SAME QUEUE IS TAKEN FOR THE NEXT ATTEMPT.!
#
#
ACTIVITY SUPERVISOR;
BEGIN
  LABEL CHECKQUEUES,NEXTELEMENTS;

```

```

{INTEGER J;
IF NOT ALLOCATORBUSY THEN
  BEGIN
    ALLOCATORBUSY+TRUE;
    J+0;
  CHECKQUEUES;
    X+FIRST(QUEUE[J]);
    IF TIMESLICE[J]>0 AND NOT EMPTY(QUEUE[J]) THEN
      BEGIN
NEXTELEMENTS:
      INSPECT X WHEN QUEUEREQUEST DO
        BEGIN
          WRITE (LN,FSEARCH,J);
          TREEBUILDTIME[RFQNUM]:=TIME(2);
          TREEBUILD;
          TREEBUILDTIME[RFQNUM]:=TIME(2)-TREEBUILDTIME
          [RFQNUM];
          WRITE (LN,FTB,RFQNUM,TREEBUILDTIME[RFQNUM]);
          WRITE;
          ALLOCATE;
          ALLOCATE;
          ALLOCATE[RFQNUM]:=RANDINT(1,500,14);
          IF NOT NOSPACE THEN
            BEGIN
              WAITTIME[RFQNUM]:=SINTIME-WAITTIME[RFQNUM];
              WRITE (LN,FALLOC,RFQNUM,WAITTIME[RFQNUM],
                J,SINTIME);
              WRITE (LN,FTD,RFQNUM,ALLOCATE[RFQNUM]);
              REMOVE(QUEUE[RFQNUM]);
              ALLOCATORBUSY+FALSE;
              ACTIVATE (QUE[RFQNUM]):=NEW JORRUNNING
              (RFQNUM,J));
            END;
          END;
        END;
      END;
      IF NOSPACE THEN
        IF X+LAST(QUEUE[J]) THEN
          BEGIN
            X+SUCC(X);
            NOSPACE+FALSE;
            GO TO NEXTELEMENTS;
          END;
        ELSE
          ALLOCATORBUSY+FALSE;
      END;
    ELSE
      BEGIN
        J+J+1;
        IF J+QUEUENUM THEN
          GO TO CHECKQUEUES;
      ELSE
        BEGIN
          FOR J+0 STEP 1 UNTIL QUEUENUM DO
            BEGIN
              TIMESLICE[J]+TIMESLICE[J]+TIMESHARD[J];
              IF TIMESLICE[J]>0 THEN
                TIMESLICE[J]+TIMESHARD[J];
              ALLOCATORBUSY+FALSE;
            END;
          QUEUEINFO;
        END;
      END;
    END;
  END;
}

```

```

    END;
END SUPERVISOR;

COMMENT THE FOLLOWING ACTIVITY SIMULATES THE HOLDING OF THE
ALLOCATED SPACE FOR A RANDOM LENGTH OF TIME. THE NEWLY ALLOCATED
REQUEST IS PUT INTO THE DOSSIER OF RUNNING JOBS AND HLD THERE
UNTIL ITS TIME, AS INDICATED BY THE RANDOM NUMBER DRAWING
PROCEDURE, IS UP. THE JOB IS THEN REMOVED FROM DOSSIER AND
THE SUPERVISOR IS ACTIVATED TO ALLOCATE ANOTHER REQUEST.;

ACTIVITY JOBRUNNING(NUM,WHICHQUEUF);
  INTEGER NUM,WHICHQUEUF;
  BEGIN
    INCLUDE (QUE[NUM],DOSSIER);  *AND PUT IN DOSSIER OF RUNNING JOBS
    INDOSSIERS;
    INQUEUES;
    RUNT1MF[NUM]+SIMTIME;
    Z+UNIFORM(0,1,U3);
    HOLD (PEAKFDRAW(5,250,100,Z));
    RUNT1MF[NUM]+SIMTIME-RUNTIME[NUM];
    WRITE (LN,FTHPU,NUM,RUNTIME[NUM]);
    REMOVE (QUF[NUM]);
    TIMES1ICE[WHICHQUEUF]+TIMES1ICE[WHICHQUEUF]-RUNTIME[NUM];
    QUFINFO;
    ACTIVATE NEW SUPERVISOR;
  END JOBRUNNING;

COMMENT THE FOLLOWING ACTIVITY RANDOMLY CHOOSES A QUEUE FOR
EACH REQUEST AND ENTERS THE REQUEST IN THE QUEUE.;

ACTIVITY QUEUEREQUEST(RFQNUM);
  INTEGER RFQNUM;
  BEGIN
    INTGFR QUENUM;
    WAITIME[RFQNUM]+SIMTIME;
    IF QUENUM=0 THEN QUENUM:=0
    ELSE QUENUM:=RANDINT(0,QUEENUM,U4);
    WRITE (LN,FORMIN,RFQNUM,QUENUM,SIMTIME);
    INCLUDE (QUE[RFQNUM],QUEUF[QUENUM]);
    INDOSSIERS;
    INQUEUES;
    ACTIVATE NEW SUPERVISOR;
  END QUEUERFQUEST;

COMMENT THE FOLLOWING ACTIVITY WAITS FOR AN AMOUNT OF SIMULATION
TIME SPECIFIED BY A RANDOM DRAWING FROM A PEAKED DISTRIBUTION,
GETS A REQUEST, AND THEN ACTIVATES ACTIVITY QUEUERFQUEST.;

ACTIVITY GTRFQUEST;
  BEGIN
    INTEGER I;
    LABEL LOOP;
    I+1;
    READEM; *THIS WILL READ SAME REQUEST OVER & OVER
  LOOP;

```

```
ACTIVATE(QUE[I]:=NEW QUEUERQUEST(I)) DFLAY 0;
I←I+1;
Z←UNIFORM(0,1,U2);
HOLD (PEAKENDDRAW(1,100,30,Z));
IF IS99 THEN
  GO TO LOOP;
END GETREQUEST;

%
%
% M A I N      P R O G R A M
U1:=54967;
U2:=34875;
U3:=4589;
U4:=678943;
ACTIVATE NEW GETREQUEST DELAY 0;
CANCEL (CURRENT);
END SIMULA;
END.
```

D-2. THE SIMULA UNTRANSLATABLE PORTION -- THE DISK
FILE ALLOCATOR AND TREEBUILD PROCEDURES, GLOBAL
DECLARATIONS AND DEFINITIONS (SIMULA/ALLOC)

This section of Appendix D contains the procedure for the allocation of disk space for the ILLIAC IV disk and other procedures, such as Treebuild, and arrays which interface with the disk file allocator and the system.

The disk file allocator in this simulator is not logically debugged. It was coded hastily by the author from system flow charts and preliminary definitions made of its arrays in an effort to get a procedure having the same interfaces with the system as was planned for the final allocator. This was because coding on this aspect of the ILLIAC IV Operating System had not begun at the time the coding on the simulator was completed.

Two other procedures are contained in this section. PROCEDURE READEM reads the data and sets up a file block. This block (logical records of 30 words each) constitutes the input to PROCEDURE TREEBUILD. PROCEDURE WRITEM outputs the results of the Treebuild procedure. These two procedures, and TREEBUILD are the property of the ILLIAC IV Operating System group.


```

* ALPHA ARRAY THING[0:97]
*
* REAL ARRAY PTRBLK [0:63,0:191],
* ASSNBLK [0:63,0:191],
* TOPBLK[0:63,0:191],
* FILBLK [0:63,0:191],
* HOLDIT[0:29]

* TREFBUILD DEFINES ARE :
*
* DEFINE NUMBPTR(NUMBPTR1)=PTRBLK[NUMBPTR1.[36:6],3xNUMBPTR1.[42:6]].
* [ 1: 9]#, 846=47.
* VPPTTR(VPPTR1)=PTRBLK[VPPTR1.[36:6],3xVPPTR1.[42:6]].
* [10:1]#,
* NUMSEGS(NUMSEGS1)=PTRBLK[NUMSEGS1.[36:6],3xNUMSEGS1.[42:6]].
* [11:21]#,
* NUMFRAGS(NUMFRAGS1)=PTRBLK[NUMFRAGS1.[36:6],3xNUMFRAGS1.[42:6]
* ].[32:16]#,
* NXTPTR(NYTPTR1)=PTRBLK[NYTPTR1.[36:6],3xNYTPTR1.[42:6]+1].
* [1:11]#,
* PHYPTR(PHYPTR1)=PTRBLK[PHYPTR1.[36:6],3xPHYPTR1.[42:6]+1].
* [12:12]#,
* VSUPTR(VSUPTR1)=PTRBLK[VSUPTR1.[36:6],3xVSUPTR1.[42:6]+1].
* [24:12]#,
* VTRKPTR(VTRKPTR1)=PTRBLK[VTRKPTR1.[36:6],3xVTRKPTR1.[42:6]+1]
* .[36:12]#,
* PHASPTR(PHASPTR1)=PTRBLK[PHASPTR1.[36:6],3xPHASPTR1.[42:6]+2]
* .[ 1:15]#, 846=47.
* CONTIGPTR(CONTIGPTR1)=PTRBLK[CONTIGPTR1.[36:6],3xCONTIGPTR1.
* [42:6]+2].[16:16]#,
* JUNKPTR(JUNKPTR1)=PTRBLK[JUNKPTR1.[36:6],3xJUNKPTR1.[42:6]+21
* .[32:16]#,
* CNT = B.[7:1]#,
* PH = B.[8:1]#,
* VFU = B.[ 9:1]#,
* VSL = B.[10:1]#,
* VTRK = B.[11:1]#,
* PFU = B.[12:1]#,
* PSU = B.[13:1]#,
* PTRK = B.[14:1]#,
* EUNUM = R.[15:4]#,
* SUNUM = R.[19:8]#,
* TRKNUIM=R.[27:10]#,
* PHS = R.[37:11]#,
* SEGS = A.[24:24]#,
* NXTFRAG(NXTFRAG1)=ASSNPLK[NXTFRAG1.[36:6],2xNXTFRAG1.[42:6]].
* [ 1:15]#, 846=47.
* NXTBL(NXTBL1)=ASSNBLK[NXTBL1.[36:6],2xNXTBL1.[42:6]].
* [16:16]#,
* SEGNUM(SEGNUM1)=ASSNPLK[SEGNUM1.[36:6],2xSEGNUM1.[42:6]+1].
* [ 1:20]#, 846=47.
* PHNUM(PHNUM1)=ASSNPLK[FHNUM1.[36:6],2xFHNU1.[42:6]+1].
* [21:11]#,
* ASSNPLKEU(ASSNPLKEU1)=ASSNPLK[ASSNPLKEU1.[36:6],3x
* ASSNPLKEU1.[42:6]+2].[1:4]#,
* ASSNPLKSU(ASSNPLKSU1)=ASSNPLK[ASSNPLKSU1.[36:6],3x
* ASSNPLKSU1.[42:6]+2].[5:4]#,
* ASSNPLKTRK(ASSNPLKTRK1)=ASSNPLK[ASSNPLKTRK1.[36:6],3x
* ASSNPLKTRK1.[42:6]+2].[9:3]#,

```

```

ASSNRLK$FG(CASSNRLK FG1)=ASSNRLK[ASSNRLK$FG1,[36:6],3x
  ASSNRLK$EG1,[42:6]+2],[12:11]#, 
  SYSLINK = HOLDIT[0],[24:24]#, 
  WDSRCD = HOLDIT[0],[19:5]#, 
  AFILNAME(AFILNAME1) = FILBLK[AFILNAME1,[36:6],6xAF$LNAMF1,
    [42:6]]#, 
  RFILNAME(RFILNAME1) = FILBLK[RFILNAME1,[36:6],6xRF$LNAMF1,
    [42:6]+1]#, 
  CFILNAME(CFILNAME1) = FILBLK[CFILNAME1,[36:6],6xCF$LNAMF1,
    [42:6]+2]#, 
  SFGSRFC0D(SEGSRFC0D1) = FILBLK[SEGSRFC0D1,[36:6],6xSEGSRFC0D1,
    [42:6]+3],[1:23]#,  *46=47. 
  TOTSEGS(TOTSEGS1) = FILBLK[TOTSEGS1,[36:6],6xTOTSEGS1,
    [42:6]+3],[24:24]#, 
  PREPTR(PREPTR1) = FILBLK[PREPTR1,[36:6],6xPREPTR1,
    [42:6]+4],[1:23]#,  *46=47. 
  P0STPTR(P0STPTR1) = FILBLK[P0STPTR1,[36:6],6xP0STPTR1,
    [42:6]+4],[24:24]#, 
  FILASSNC(FILASSN1) = FILBLK[FILASSN1,[36:6],6xFILASC1,[42:6]
    +5],[1:11]#,  *46=47. 
  PHYSICALFU(PHYSICALFU1)=TOPBLK[PHYSICALFU1,[36:6],2x
    PHYSICALFU1,[42:6]], [1:9]#, 
    VIRTUALFU(VIRTUALFU1)=TOPBLK[VIRTUALFU1,[36:6],2x
    VIRTUALFU1,[42:6]], [10:12]#, 
  PHYSICALSU(PHYSICALSU1)=TOPBLK[PHYSICALSU1,[36:6],2x
    PHYSICALSU1,[42:6]], [46:1]#, 
  PHYSICALTRK(PHYSICALTRK1)=TOPBLK[PHYSICALTRK1,[36:6],2x
    PHYSICALTRK1,[42:6]], [47:1]#, 
  VIRTUALSU(VIRTUALSU1)=TOPBLK[VIRTUALSU1,[36:6],2x
    VIRTUALSU1,[42:6]], [22:12]#, 
  VIRTUALTRK(VIRTUALTRK1)=TOPBLK[VIRTUALTRK1,[36:6],2x
    VIRTUALTRK1,[42:6]], [34:12]#, 
  PHASEDPTR(PHASEDPTR1)=TOPBLK[PHASEDPTR1,[36:6],2x
    PHASEDPTR1,[42:6]+1],[1:15]#, 
  C0NTGPTR(C0NTGPTR1)=TOPBLK[C0NTGPTR1,[36:6],2x
    C0NTGPTR1,[42:6]+1],[16:16]#, 
  JNKPTR(JNKPTR1)=TOPBLK[JNKPTR1,[36:6],2x
    JNKPTR1,[42:6]+1],[32:16]#, 
  ASEGSRECD = HOLDIT[7],[1:23]#,  *46=47. 
  ATOTSEGS = HOLDIT[7],[24:24]#, 
  APRFFTR = HOLDIT[8],[1:23]#,  *46=47. 
  APOSTPTR = HOLDIT[8],[24:24]#;

```

9
% PROCEDURE ALLOCATE-CREATED ARRAYS ARE:

9
%
REAL AFARRAY MAPBLKPTRARRA[0:63,0:191],
MAPBLK[0:63,0:191],
MAPSEG[0:1027];

9
% ALLOCATE OFFINES ARE:

9
DEFINE NUMSUFRAGS(NUMSUFRAGS1,NUMSUFRAGS2)=MAPBLKPTRARRA[NUMSUFRAGS1,
NUMSUFRAGS2],[1:12]#.
NUMAVAILSUSEGS(NUMAVAILSUSEGS1,NUMAVAILSUSEGS2)=MAPBLKPTRARRA
[NUMAVAILSUSEGS1,NUMAVAILS1SFGS2],[13:13]#,
WHICHMAPNUM(WHICHMAPN1,WHICHMAPNUM2)=MAPBLKPTRARRA[WHICHMAPNUM1,
WHICHMAPNUM2],[26:14]#,
MEU(MEU1)=MAPBLK[MEU1,[36:6],MEU1,[42:6]], [1:4]#,
MSU(MSU1)=MAPBLK[MSU1,[36:6],MSU1,[42:6]], [5:4]#,
MLOCK(MLOCK1)=MAPBLK[MLOCK1,[36:6],MLOCK1,[42:6]], [9:1]#,


```

* IS ENTERED INTO THE NEW REQUEST. IF THIS IS THE FIRST ASSNBLK FOR
* A FILE, THE ASSNBLK # IS ENTERED INTO THE FILE BLK FOR THAT FILE.
* WCH = CASE SWITCH.
*****ASSNBLK*****  

PROCEDURE ASSN(WCH);
  INTEGER WCH;
  BEGIN
    INTEGER PP, QP, LASTONE;
    LABEL FILL1, FILL2, OTRO, FIN2;
    LASTONE:=0;
* LOOK AT THE PHASE, CONTIG, OR JUNK PTR OF THE LOWEST
* LEVEL BLK NECESSARY FOR THIS REQUEST.
CASE WCH OF
  FEGLIN
    PH := PHASPTR(NN);
    FP := CONTIGPTR(NN);
    PP := JUNKPTR(NN);
  END;
* IF THE PCJ PTR IN THE LEVEL BLOCK IS NULL CREATE THE NEW
* ASSIGNMENT BLK AND SET THE PCJ PTR TO POINT TO IT.
  IF PP = 0 THEN GO TO FILL1;
  OTRO:
* IF NO. OF SEGMENTS IN ASSNBLK POINTED TO IS > NEW GUY S
* NO. OF SEGS, LOOK AT NXT ASSNBLK & COMPARE NO. OF SEGS.
  IF SEGNUM(PP) > SEGS THEN
    BEGIN
      %GET PTR TO NEXT ASSNBLK
      QP := NXTEL(PP);
      IF QP NEQ 0 THEN
        BEGIN
          LASTONE + PP;
          PP + QP;
          GO TO OTRO;
        END
      ELSE
        % CREATE NEW ASSNBLK AT END OF LIST OF OLD ASSNBLKS.
        BEGIN
          NXTEBL(PP) + NXASSN; %POINT LASTONE ASSNBLK TO NEW.
          SEGNUM(NXASSN)+SEGS; %ENTER NO. OF SEGS INTO NEW.
          FNUM(NXASSN)+FHS; %ENTER NO. OF PHASES.
          %IF THIS IS THE FIRST ASSNBLK FOR A FILE.
          %POINT THE FILE BLK TO IT.
          IF LASTONE=0 THEN FTASSN(NXFILE):=NXASSN ELSE
            NXTEBL(LASTONE)+NXASSN; %POINT LAST CREATED TO NEW.
          LASTONE:=NXASSN;
          NXASSN + NXASSN + 1;
          GO TO FIN2;
        END
    END
  ELSE %INTERLEAVE NEW ASSNBLK IN OLD LIST.
    BEGIN
      NXTEBL(NXASSN) + PP;
      % IF THIS IS THE FIRST ASSNBLK OF THIS TYPE FOR THIS
      % LEVEL BLK, POINT THE LEVEL BLK TO IT ELSE POINT THE
      % PRECEEDING ASSNBLK TO IT.
      IF LASTONE NEQ 0 THEN NXTEBL(LASTONE):=NXASSN ELSE
        % POINT THE PHASE, CONTIG, OR JUNK PTR IN THE
        % LEVEL BLK TO THE ASSNBLK.
      CASE WCH OF
        BEGIN
          PHASPTR(NN) := NXASSN;
        END
      END
    END
  FIN2:

```

```

        COUNTIGPTR(NN) != NXASSN;
        JUNKPTR(NN) != NXASSN;
    END;
    GO TO FILL2;
END;
FIN2:END ASSN;
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
* FIND CREATES A NEW LEVEL BLK (BLK P) ACCORDING TO A REQUEST AND
* PTS THE ASSOCIATED BLK ON THE LFVEL ABOVE IT (BLK A) TO THE NEW
* LEVEL BLK.
* FIND IS ENTERED WITH RM CONTAINING THE LFVFI BLK NO. OF BLK A,
* AND WCH INDICATING WHICH PTR SHOULD BE TAKEN FROM BLK A.
* UPON EXIT FROM FIND, NN CONTAINS THE LFVFI BLOCK NO. OF BLK B,
* ASSOCIATED WITH EACH PTRNTER IN BLK A, IS / LIST OF LFVFL BLKS
* OF COMMON TYPE (E.G. FUD,SU,TRK) IN THE ORDER IN WHICH THEY WERE
* CREATED, (LAST CREATED AT END OF LIST).
* THIS PROCEDURE LOOKS DOWN THE LIST AND 3 CASES CAN ARRISE...
* 1. THE LIST IS FMPTY.
*           ACTION
*           A NEW LFVEL BLK IS CREATED AND THE CORPES. PTR IN BLK A
*           IS SET TO POINT TO IT.
* 2. IT FINDS A LEVEL BLK IN THE LIST WITH THE SAME NO.
*     (I.E. FUD,SU,TRK #).
*           ACTION
*           NO NEW BLK IS CREATED.
* 3. IT FINDS NO LEVEL BLK IN THE LIST WITH THE SAME NO.
*           ACTION
*           A NEW LFVEL BLK IS CREATED AND "NXT BLK" PTR OF THE OLD
*           "BOTTOM OF THE LIST" LEVEL BLK IS SET TO PT TO NEW BLK
*           IN ALL CASES, NN IS ENTERED INTO AN ARRAY WHICH CONTAINS THE NO.S
*           OF ALL LEVEL BLKS ASSOCIATED WITH THE PRESENT REQUEST.
*           NM = FUD, SU, OR TRK NUMBER.
*           TR = EXIT SWITCH.
*           WCH = CASF SWITCH.
*           VP = VIRTUAL PHYSICAL FLAG (1 IF PHYSICAL, 0 IF VIRTUAL).
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
PROCEDURE FIND(LNXT,NUM,TR,WCH,VP);
    VALUE NUM;
SWITCH LNXT;
    INTEGER NUM,TR,WCH,VP;
    PFG1;
    INTEGER MM,NM;
    ALUFAN FIRST1;
    LABFI NFU1,NXNT;
    NM := NN;
* GET THE PTR TO THE NEXT LEVEL AS REQUIRED BY THE REQUEST.
CASE WCH OF
    REGIN
        NM := PHYPTR(NM);
        NM := NXTPTR(NM);
        NM := VSUPTR(NM);
        NM := VTRKPTR(NM);
    END;
*IF THE PTR IS NULL CREATE A NEW ELOCK.
    IF NM = 0 THEN
        REGIN
        FIRST1 := TRUE;
        GO TO NEWU;
    END;
NXNT:
*IF FUD,SU,TRK# AGREE, YOU VE GOT NN...EXIT FIND.

```



```

I != 1;
GO TO LP9;
END;
I != 9;
* READ FILE NAME INTO NEXT FILE BLOCK.
REPLACE(CFILENAME(NXFIL),0,HOLDIT[1],0,1);
REPLACE(PFILENAME(NXFIL),0,HOLDIT[2],0,1);
REPLACE(CFILENAME(NXFIL),0,HOLDIT[3],0,1);
* READ IN NO. OF SEGS/RECD AND TOTAL NO. OF SEGS FOR THIS FILE.
SEGSRECD(NXFIL) + ASFGSRECD;
TOTSEGS(NXFIL) + ATOTSEGS;
* ENTER POST AND PRE PROCESS LOCATIONS INTO FILE BLK.
FREPTR(NXFIL) + APREPTR;
FOPTPTR(NXFIL) + APOSTPTR;
* IF YOU HAVE PROCESSED ALL 29 REQUESTS IN THIS PHYSICAL RECORD
* GO GET ANOTHER UNF.
LP9: IF I = 29 THEN
  BEGIN
    TOP := FALSE;
    GO TO RD;
  END;
* INITIALIZE NN TO POINT TO TOP BLK.
NN := 1;
* INITIALIZE ADDSEGS ARRAY INDEX TO 0.
AS := 0;
A1:=HOLDIT[1];
F1:=HOLDIT[1+1];
* IF THIS IS THE END OF THIS FILE, SEE IF THERE ARE OTHER FILES.
IF A = 0 AND F = 0 THEN
  * IF THERE IS ANOTHER FILE PREPARE TO FORM FILE BLOCK.
  IF NXFT = 0 THEN GO TO FIN4 ELSE
    BEGIN
      TOP := TRUE;           * INDICATE NEW FILE READ.
      NXFT := NXFT + 1;      * POINT TO NEXT FILE BLK.
      LASTIN := 0;           * INITIALIZE LASTIN.
      GO TO RD;
    END;
* IF A PHYSICAL FU IS NOT REQUIRED GO TO LVFU.
IF PFU = 0 THEN GO TO LVFSU;
FIND(LNXT,FLNUM,0,0,1);

LPTRK:
* IF A PHYSICAL TRK IS NOT REQUIRED, GO TO LVTRK.
IF FTRK = 0 THEN GO TO LVTRK;
FIND(LNXT,TRKNUM,2,0,1);

LVFSU:
* IF A VIRTUAL FU NOT REQUIRED GO TO LVSH.
IF VFL = 0 THEN GO TO LVSH;
FIND(LNXT,FLNUM,1,0,1);

LVSH:
* IF A VIRTUAL SU IS NOT REQUIRED GO TO LVTRK.
IF VSU = 0 THEN GO TO LVTRK;
FIND(LNXT,SUNUM,1,2,0);

LVTRK:
* IF A VIRTUAL TRK IS NOT REQUIRED GO TO FINL.
IF VTRK = 0 THEN GO TO FIN3;
FIND(LNXT,TRKNUM,2,3,0);

FIN3:

```



```

MAPPTR(WHICHMAP):=NEXTMAPBLOCK(THISMAP);
FREEMAPSPACE (THISMAP);
NMAPFRAGMENTS(WHICHMAP):=NMAPFRAGMENTS(WHICHMAP)+1;
GO TO FIN;
END;
ELSIF
BEGIN
  IF PHASE+SEGNUM(ASSNBLKPTR) NEQ FIRSTSEG(THISMAP)+NUMSEG
  (THISMAP) THEN
    BEGIN
      NEWMAP:=NEXTMAPBLOCK(THISMAP);
      GETMAPSPACE (NEWMAP);
      FIRSTSEG(NEWMAP):=PHASE+SEGNUM(ASSNPLKPTR);
      NUMSEG(NEWMAP):=FIRSTSEG(THISMAP)+NUMSEG(THISMAP)-
      FIRSTSEG(NEWMAP);
      NXXTMAPBLOCK(NEWMAP):=NXXTMAPBLOCK(THISMAP);
      NXXTMAPBLOCK(THISMAP):=NEWMAP;
      NMAPFRAGMENTS(WHICHMAP):=NMAPFRAGMENTS(WHICHMAP)+1;
    END;
    NUMSEG(THISMAP):=PHASE-FIRSTSEG(THISMAP);
  END;
END;
FIN:
END ASSIGN;
*
*
*
INTEGER PROCEDURE RELEASE(ASSNPLKPTR,WHICHMAP);
INTEGER ASSNRLKPTR,WHICHMAP;
BEGIN
  INTEGER PHASE,TOTALSEG,NEXTMAP,MAPADDR,NEWMAP;
  LABEL FIN,LOOP;
  NUMSEGINMAP(WHICHMAP):=NUMSEGINMAP(WHICHMAP)+SEGNUM(ASSNBLKPTR);
  PHASE:=ASSNPLKTRK(ASSNBLKPTR)*NUMSEGSPRTRK+ASSNPLKSEG
  (ASSNPLKPTR);
  TOTALSEG:=SEGNUM(ASSNRLKPTR);
  NXXTMAP:=MAPADDR:=MAPPTR(WHICHMAP);
LOOP:
  IF NXXTMAP=0 OR PHASE+TOTALSEG LSS FIRSTSEG(NEXTMAP) THEN
    BEGIN
      GETMAPSPACE (NEWMAP);
      FIRSTSEG(NEWMAP):=PHASE;
      NUMSEG(NEWMAP):=TOTALSEG;
      NXXTMAPBLOCK(NEWMAP):=NXXTMAP;
      NMAPFRAGMENTS(WHICHMAP):=NMAPFRAGMENTS(WHICHMAP)+1;
      IF MAPADDR=0 THEN
        DO
          BEGIN
            MAPADDR:=NXXTMAPBLOCK(MAPADDR);
            NXXTMAPBLOCK(MAPADDR):=NXXTMAP;
          END
        UNTIL NXXTMAPBLOCK(MAPADDR)=NXXTMAP;
      ELSE
        MAPPTR(WHICHMAP):=NXXTMAP;
      RELEASE:=NEWMAP;
      GO TO FIN;
    END;
  END;
ELSIF
  BEGIN
    IF PHASE+TOTALSEG NEQ FIRSTSEG(NEXTMAP) THEN
      IF PHASE=FIRSTSEG(NEXTMAP)+NUMSEG(NEXTMAP) THEN
        IF NXXTMAPBLOCK(NEXTMAP) NEQ 0 THEN

```

```

BEGIN
  IF FIRSTSEG(NEXTMAP)+NUMSEG(NEXTMAP)+TOTALSEG
  =FIRSTSEG(NEXTMAPLOCK(NEXTMAP)) THEN
    BEGIN
      NUMSEG(NEXTMAP):=NUMSEG(NEXTMAP)+TOTALSEG+
      NUMSEG(NEXTMAPLOCK(NEXTMAP));
      NEXTMAPLOCK(NEXTMAP):=NEXTMAPLOCK
      (NEXTMAPLOCK(NEXTMAP));
      FREEMAPSPACE(NEXTMAPLOCK(NEXTMAP));
      NMAPFRAGMENTS(WHICHMAP):=
      NMAPFRAGMENTS(WHICHMAP)-1;
    END;
  END;
ELSE
  IF RFGTN
  THEN
    NEXTMAP:=NEXTMAPLOCK(NEXTMAP);
    GO TO LOOP;
  END;
ELSE
  FIRSTSEG(NEXTMAP):=PHASE;
  NUMSEG(NEXTMAP):=NUMSEG(NEXTMAP)+TOTALSEG;
  RELEASESF:=NEXTMAP;
  END;
FIN:
  END RELEASESF;
*
*
*
PROCEDURE ALLOCJUNK (ASSNBLKPTR,WHICHMAP);
  INTEGER ASSNBLKPTR,WHICHMAP;
BEGIN
  INTEGER NEWASSNBLK,NBLOCKS;
  IF ASSNBLKPTR NEQ 0 THEN
    BEGIN
      NBLOCKS:=MAPPTR(WHICHMAP);
      IF NUMSEG(NBLOCK)<SEGNUM(ASSNBLKPTR) THEN
        BEGIN
          NEWASSNBLK:=NXTBL(ASSNBLKPTR);
          GFTASSNBLKSPACE (NEWASSNBLK);
          NXTBL(NEWASSNBLK):=NXTBL(ASSNBLKPTR);
          NXTFRAG(NEWASSNBLK):=NXTFRAG(ASSNBLKPTR);
          NXTBL(ASSNBLKPTR):=NEWASSNBLK;
          NXTFRAG(ASSNBLKPTR):=NEWASSNBLK;
          SEGNUM(NEWASSNBLK):=SEGNUM(ASSNBLKPTR)-NUMSEG(NBLOCK);
          SEGNUM(ASSNBLKPTR):=NUMSEG(NBLOCK);
        END;
      ASSIGN (ASSNBLKPTR,WHICHMAP,FIRSTSEG(NBLOCK),NBLOCK);
      ALLOCJUNK (NXTBL(ASSNBLKPTR),WHICHMAP);
    END;
  END ALLOCJUNK;
*
*
*
BOOLEAN PROCEDURE ALLOCCONTIG(ASSNBLKPTR,WHICHMAP);
  INTEGER ASSNBLKPTR,WHICHMAP;
BEGIN
  INTEGER NBLOCKS;
  LABEL LOOP,FIN;
  IF ASSNBLKPTR#0 THEN
    BEGIN
      NBLOCKS:=MAPPTR(WHICHMAP);

```

```

LOOP1:
    IF NBLOCK#0 THEN
        IF NUMSEG(NBLOCK)>=SEGNUM(ASSNBLKPTR) THEN
            BEGIN
                ASSIGN(ASSNBLKPTR,WHICHMAP,FIRSTSEG(NBLOCK),NBLOCK);
                IF ALLOCCONTIG(NXTBL(ASSNBLKPTR),WHICHMAP)
                THEN
                    BEGIN
                        ALLOCCONTIG:=TRUE;
                        GO TO FIN;
                    END
                ELSE
                    BEGIN
                        NBLOCK:=NEXTMAPBLOCK(RLEASESR(ASSNBLKPTR,
                            WHICHMAP));
                        GO TO LOOP1;
                    END;
                END;
            FND
        ELSE
            BEGIN
                NBLOCK:=NEXTMAPBLOCK(NBLOCK);
                GO TO LOOP1;
            END;
        END;
    ELSE
        BEGIN
            ALLOCCONTIG:=FALSE;
            GO TO FIN;
        END;
    END;
    ELSE
        BEGIN
            ALLOCCONTIG:=TRUE;
        END;
FIN:
    END ALLOCCONTIG;
*
*
*
BOOLEAN PROCEDURE PALLOC (PHASE1,ASSNBLKPTR,WHICHMAP);
    VALUE PHASE1,ASSNBLKPTR,WHICHMAP;
    INTEGER PHASE1,ASSNBLKPTR,WHICHMAP;
    BEGIN
        INTEGER NEXTMAP,PHASE;
        LABEL LOOP1,LOOP2,F1NTRUE,F1NFALSE,FIN;
LOOP1:
    IF ASSNBLKPTR#0 THEN
        BEGIN
            NEXTMAP:=MAPPTR(WHICHMAP);
            PHASE:=PHASE1+PHNUM(ASSNBLKPTR) MOD NUMSEGSPTRK;
            IF NEXTMAP#0 THEN
                BEGIN
                    IF FIRSTSEG(NEXTMAP)<=PHASE THEN
                        IF FIRSTSEG(NEXTMAP)+NUMSEG(NEXTMAP)<PHASE THEN
                            BEGIN
                                NEXTMAP:=NEXTMAPBLOCK(NEXTMAP);
                                GO TO LOOP1;
                            END
                        ELSE
                            BEGIN
                                IF FIRSTSEG(NEXTMAP)+NUMSEG(NEXTMAP)>=PHASE+SEGNUM
                                    (ASSNBLKPTR) THEN
                                    BEGIN

```

```

ASSIGN(CASSNBLKPTR,WHICHMAP,PHASE,NEXTMAP);
IF PALLOC(PHASE1,NXTBL(CASSNBLKPTR),
WHICHMAP) THEN
    GO TO FINTRUE
ELSE
    NEXTMAP:=RELEASE(CASSNBLKPTR,WHICHMAP);
END;
IF PHASE GEQ NUMSEGINMAP(WHICHMAP) THEN
    GO TO FINFALSE
ELSE
    GO TO LOOP1;
END;
ELSIF
    BEGIN
        PHASE:=PHASE+NUMSEGSPFRTRK;
        IF PHASE=NUMSEGINMAP(WHICHMAP) THEN
            GO TO FINFALSE
        ELSE
            GO TO LOOP2;
    END;
    ELSE
        GO TO FINFALSE;
    END;
GO TO FINTRUE;
END;
FINTRUE: PALLOC+TRUE;
GO TO FIN;
FINFALSE: PALLOC+FALSE;
FIN:
    END PALLOC;
*
*
*
BOOLEAN PROCEDURE ALLOCPHASED(CASSNBLKPTR,WHICHMAP);
INTEGERR ASSNBLKPTR,WHICHMAP;
BEGIN
    INTEGER NBLLOCK,PHASE;
    LABEL LOOP,FIN;
    NBLLOCK:=MAPPTR(WHICHMAP);
LOOP:
    PHASE+FIRSTSEG(NBLLOCK);
    IF NOT PALLOC(PHASE,CASSNBLKPTR,WHICHMAP) THEN
        BEGIN
            NBLLOCK+NEXTMAPBLOCK(NBLLOCK);
            IF NBLLOCK#0 THEN
                GO TO LOOP;
            ELSE
                BEGIN
                    ALLOCPHASED+FALSE;
                    GO TO FIN;
                END;
        END;
    ELSE
        ALLOCPHASED+TRUE;
    END;
FIN:
    END ALLOCPHASED;
*
*
*
BOOLEAN PROCEDURE ALLOCABSPHASER (CASSNBLKPTR,WHICHMAP);
INTEGERR ASSNBLKPTR,WHICHMAP;
BEGIN

```

```

INTEGER NRLOCK, PHASE, SIZE;
LABEL LOOP, FIN, FINTRUE;
IF ASSNBLKPTR#0 THEN
  BEGIN
    NBLOCK+MAPPTR(WHICHMAP);
    PHASE:=PHNUM(ASSNBLKPTR);
    SIZE+SEGNUM(ASSNBLKPTR);
  LOOP:
    IF NBLOCK#0 THEN
      IF FIRSTSEG(NBLOCK)≤PHASE THEN
        IF FIRSTSEG(NBLOCK)+NUMSEG(NBLOCK)≥PHASE+SIZE THEN
          BEGIN
            ASSIGN(ASSNPLKPTR, WHICHMAP, PHASF, NRLOCK);
            IF ALLOCABSPHASED(NXTBL(ASSNPLKPTR),
              WHICHMAP) THEN
              GO TO FINTRUE;
            ELSE
              RFLEASER(ASSNPLKPTR, WHICHMAP);
          END
        ELSE
          BEGIN
            NRLOCK+NFXTMAPBLOCK(NBLOCK);
            GO TO LOOP;
          END;
        ALLOCABSPHASFD+FALSE;
      END;
    FINTRUE:
      ALLOCABSPHASED:=TRUE;
    END ALLOCABSPHASED;
  END;
  PROCEDURE DEALLOCATELIST(PTR);
  INTEGER PTR;
  IF PTR NEQ 0 THEN
    BEGIN
      RELEASER(PTR, WHICHMAPNUM(ASSNPLKFI(PTR)),
        ASSNBLKSI(PTR));
      DEALLOCATELIST(NXTBL(PTR));
    END DEALLOCATELIST;
  PROCEDURE DEALLOCATETRK(PTR);
  INTEGER PTR;
  IF PTR NEQ 0 THEN
    BEGIN
      DEALLOCATELIST(PHASEDPTR(PTR));
      DEALLOCATELIST(CONTGPTR(PTR));
      DEALLOCATELIST(JNKPTR(PTR));
      DEALLOCATETRK(NXTPTR(PTR));
    END DEALLOCATETRK;
  PROCEDURE DEALLOCATESU(PTR);
  INTEGER PTR;
  IF PTR NEQ 0 THEN
    BEGIN
      DEALLOCATETRK(PHYSICALTRK(PTR));
      DEALLOCATETRK(VIRTUALTRK(PTR));
    END;
  END;

```

```

DEALLOCATELIST(PHASEDPTR(PTR));
DEALLOCATELIST(CONTGPTR(PTR));
DEALLOCATELIST(JNKPTR(PTR));
DEALLOCATESU(NXTPTR(PTR));
END DEALLOCATESU;

* * *
* * *
* * *

PROCEDURE DEALLOCATEEU(PTR);
INTEGER PTR;
IF PTR NEQ 0 THEN
  BEGIN
    DEALLOCATESU(PHYSICALSU(PTR));
    DEALLOCATESU(VIRTUALSU(PTR));
    DEALLOCATEFTP(VIRTUALTRK(PTR));
    DEALLOCATELIST(PHASEDPTR(FTR));
    DEALLOCATELIST(CONTGPTR(PTR));
    DEALLOCATELIST(JNKPTR(PTR));
    DEALLOCATEEU(NXTPTR(PTR));
  END DEALLOCATEEU;

* * *
* * *
* * *

PROCEDURE DEALLOCATEDISK;
BEGIN
  DEALLOCATEEU(PHYSICALEU(TOPLOCK));
  DEALLOCATEEU(VIRTUALEU(TOPLOCK));
  DEALLOCATESU(VIRTUALSU(TOPLOCK));
  DEALLOCATETRK(VIRTUALTRK(TOPLOCK));
  DEALLOCATELIST(PHASEDPTR(TOPLOCK));
  DEALLOCATELIST(CONTGPTR(TOPLOCK));
  DEALLOCATELIST(JNKPTR(TOPLOCK));
END DEALLOCATEDISK;

* * *
* * *
* * *

PROCEDURE FUSIJUNKALLOC(ASSNPLKPTR,FIRSTEU,LASTEU,FIRSTSU,LASTSU);
INTEGER ASSNPLKPTR,FIRSTEU,LASTEU,FIRSTSU,LASTSU;
BEGIN
  INTEGER NPLOCK,WHICHMAP,EU,SU;
  LARFL(FIN);
  INTGFR(NEWASSNBLK);
  IF ASSNPLKPTR#0 THEN
    BEGIN
      FOR EU<FIRSTEU STEP (IF FIRSTEU=LASTEU THEN 1 ELSE -1) UNTIL
      LASTEU DO
        BEGIN
          WHICHMAP:=MAPRLKPTRARRAY(EU,SU);
          NPLOCK:=MAPPTR(WHICHMAP);
          IF NUMSEGINMAP(WHICHMAP)#0 THEN
            BEGIN
              IF NUMSEG(NPLOCK)<SEGNUM(ASSNPLKPTR) THEN
                BEGIN
                  GETASSNPLKSPACE(NEWASSNBLK);
                  NXTBL(NEWASSNBLK):=NXTBL(ASSNPLKPTR);
                  NXTBL(ASSNPLKPTR):=NEWASSNBLK;
                  SEGNUM(NEWASSNBLK)+SEGNUM(ASSNPLKPTR)-
                  NUMSEG(NPLOCK);
                  SEGNUM(ASSNPLKPTR)+NUMSEG(NPLOCK);
                END;
            END;
        END;
    END;
  END;

```

```

ASSIGN(ASSNBLKPTR,WHICHMAP,FIRSTSFG(NRLOCK),NBLOCK))
NUMSEGINMAP(WHICHMAP)+NUMSEGINMAP(WHICHMAP)-SENUM
(ASSNBLKPTR)
GO TO FIN
ENDS
ENDS
ERROR TERMINATION
ENDS
FIN:
END EUSUJUNKALLOC

%
%
%
BOOLEAN PROCEDURE EUSUCONTIGALLOC(ASSNBLKPTR,FIRSTEU,LASTEU,FIRSTSU,
LASTSU);
INTEGER ASSNBLKPTR,FIRSTEU,LASTEU,FIRSTSU,LASTSU;
BEGIN
INTEGER NRLOCK,WHICHMAP,EUSU;
LABEL FINTRUE,LOOP,FTM;
IF ASSNBLKPTR=0 THEN
EUSUCONTIGALLOC+TRUE;
ELSE
FOR EU+FIRSTEU STEP (IF FIRSTEU LEQ LASTEU THEN 1
ELSE -1) UNTIL LASTEU DO
FOR SU+FIRSTSU STEP 1 UNTIL LASTSU DO
BEGIN
WHICHMAP:=MAPRLKPTRARRAY(EU,SU);
NRLOCK+MAPPTR(WHICHMAP);
IF NUMSEGINMAP(WHICHMAP)>SENUM(ASSNBLKPTR) THEN
LOOP:
IF NRLOCK#0 THEN
IF NUMSEG(NRLOCK)>SENUM(ASSNBLKPTR) THEN
BEGIN
ASSIGN(ASSNBLKPTR,WHICHMAP,FIRSTSFG(NRLOCK),
NRLOCK);
NUMSEGINMAP(WHICHMAP)+NUMSEGINMAP(WHICHMAP)=
SENUM(ASSNBLKPTR);
IF EUSUCONTIGALLOC(NXTBL(ASSNBLKPTR
),LASTEU,FIRSTEU,FIRSTSU,LASTEU) THEN
GO TO FINTRUE;
NRLOCK+NEXTMAPBLOCK(REALSER(ASSNBLKPTR,
WHICHMAP));
NUMSEGINMAP(WHICHMAP)+NUMSEGINMAP(WHICHMAP)+
SENUM(ASSNBLKPTR);
GO TO LOOP;
END;
ELSE
BEGIN
NRLOCK+NEXTMAPBLOCK(NRLOCK);
GO TO LOOP;
END;
END;
EUSUCONTIGALLOC+FALSE;
GO TO FIN;
FINTRUE: EUSUCONTIGALLOC+TRUE;
FIN:
END EUSUCONTIGALLOC;
%
%
%
BOOLEAN PROCEDURE ALLOCATPHASED(PHASEDPTR,FLOCKPTR);

```

```

INTEGER PHASEDPTR,BLOCKPTR
BEGIN
ENDS

*
*
*
BOOLEAN PROCEDURE ALLOCATONTRK(FIRSTEU,LASTEU,FIRSTSU,LASTSU,
BLOCKPTR)
  INTEGER FIRSTEU,LASTEU,FIRSTSU,LASTSU,BLOCKPTR
  BEGIN
    FORMAT FALLOCATONTRK ("ERROR IN TRACK ALLOCATION. ALLOCATION ",
      "TERMINATED.")
    IF BLOCKPTR=0 THEN
      ALLOCATONTRK:=TRUE
    ELSE
      END ALLOCATONTRK
  *
  *
  *
BOOLEAN PROCEDURE ALLOCATONSU(FIRSTEU,LASTEU,BLOCKPTR)
  INTEGER FIRSTEU,LASTEU,BLOCKPTR
  BEGIN
    INTEGER WHICHMAP,SU,EU,FIRSTSU,LASTSU
    LABEL FIN
    IF BLOCKPTR NEQ 0 THEN
      BEGIN
        IF VPPTR(BLOCKPTR)=0 THEN
          FIRSTEU=LASTEU=NUMBPTR(BLOCKPTR)
        ELSE
          BEGIN
            FIRSTSU:=FIRSTSUNUM;
            LASTSU:=LASTSUNUM;
          END;
        FOR EU:=FIRSTEU STEP 1 UNTIL LASTEU DO
          FOR SU:=FIRSTSU STEP 1 UNTIL LASTSU DO
            BEGIN
              WHICHMAP:=MAPBLKPTRARRAY(EU,SU);
              IF NOT (MLOCK(WHICHMAP)=0 OR NUMSEGS(BLOCKPTR) LSS
                NUMSEGTMAP(WHICHMAP)) THEN
                BEGIN
                  IF ALLOCATONTRK(EU,EU,SU,SU,PHYSICAL TRK(BLOCKPTR))
                    THEN
                    BEGIN
                      IF ALLOCATEPHASED(PHASEDPTR(BLOCKPTR),
                        WHICHMAP) THEN
                        BEGIN
                          IF ALLOCCONTIG(CONTIGPTR(BLOCKPTR),
                            WHICHMAP) THEN
                            BEGIN
                              ALLOCJUNK(JUNKPTR(BLOCKPTR),
                                WHICHMAP);
                              IF VPPTR(BLOCKPTR)=0 THEN
                                BEGIN
                                  MLOCK(WHICHMAP):=1;
                                  NUMAVAILSUSFGS(EU,SU):=
                                    NUMAVAILSUSFGS(EU,SU)-NUMSEGS
                                    (BLOCKPTR);
                                END;
                              IF ALLOCATONSU(FIRSTEU,LASTEU,
                                NEXTPTR(BLOCKPTR)) THEN
                                BEGIN

```



```

(BLOCKPTR),FU,SU,FIRSTSUNUM,
LASTSUNUM) THEN
BEGIN
  FUSUJUNKALOC(JUNKPTR(BLOCKPTR)
  ,EU,SU,FIRSTSUNUM,LASTSUNUM);
  IF VPPTR(BLOCKPTR)=1 THEN
    BEGIN
      MLOCK(WHICHMAP):=1;
      NUMAVAILSEGSC(FU,SU):=
      NUMAVAILSEGSC(EU,SU)-
      NUMSEGSC(BLOCKPTR);
    END;
    IF ALLOCATEONFU(NXTPTP(BLOCK PTR)
    ) THEN
      GO TO FINTRUE;
  ELSE
    BEGIN
      DEALLOCATELIST(JUNKPTR
      (BLOCKPTR));
      DEALLOCATELIST(COM1GPTH
      (BLOCKPTR));
      MLOCK(WHICHMAP):=0;
      NUMAVAILSEGSC(FU,SU):=
      NUMAVAILSEGSC(EU,SU)-
      NUMSEGSC(BLOCKPTR);
    END;
    ENDS;
    DEALLOCATELTST(PHASEDPTR(BLOCKPTR));
    DEALLOCATETRK(VIRTUALTRK(BLOCKPTR));
  ENDS;
  DEALLOCATESU(VIRTUALSU(BLOCKPTR));
  ENDS;
  DEALLOCATESU(PHYSICALSU(BLOCKPTR));
END;
  ALLOCATEONEU:=FALSE;
  GO TO FIN;
END;
FINTRUE:
  ALLOCATEONFU:=TRUE;
FIN:
  END ALLOCATEONFU;
}
}
}

BOOLEAN PROCEDURE ALLOCATEONDISK;
BEGIN
  INTGFF EU,SU;
  LABEL FIN,JUMP;
  IF NUMSEGSC(TOPBLOCK) LFO AMOUNTOFFREDISK THEN
    IF ALLOCATEONEU(PHYSICALFU(TOPBLOCK)) THEN
      IF ALLOCATEONFU(VIRTUALFU(TOPBLOCK)) THEN
        BEGIN
          IF ALLOCATONSU(FIRSTEUNUM,LASTEUNUM,VIRTUALSU
          (TOPBLOCK)) THEN
            BEGIN
              IF ALLOCATEONTRK(FIRSTEUNUM,LASTEUNUM,FIRSTSUNUM,
              LASTSUNUM,VIRTUALTRK(TOPBLOCK)) THEN
                BEGIN
                  FOR FU:=FIRSTEUNUM STEP 1 UNTIL LASTEUNUM DO
                  FOR SU:=FIRSTSUNUM STEP 1 UNTIL LASTSUNUM
                  DO

```



```

ANN[0],[24:24] := LINK := B;
FILL ZEROUTE[*] WITH "0000000000";
IF ANN[27] NEQ 0 AND ANN[28] NEQ 0 THEN
  BEGIN
    FOR CNT := 1 STEP 1 UNTIL 3 DO
      RFPLACE(ANN[CNT],0,ZEROUTE[*],0,1);
    ZB := 13;
    QT := 13;
    GO TO LBLKS;
  END;
ZB := QT := 0;
READ(INN,3,ANP[*]);
  REPLACF(ANN[*],8,ANP[*],0,3);
FOR CNT := 0 STEP 1 UNTIL 1 DO
  BEGIN
    READ(INN,FF,A,R);
    ANN[7+CNT].[1:23] := A;
    ANN[7+CNT].[24:24] := R;
  END;
LBLKS: FOR CNT := 0 STEP 1 UNTIL ZB DO
  BEGIN
    READ(INN,FF,A,R);
    ANN[QT+2*cnt].[1:23] := A;
    ANN[QT+2*cnt].[24:24] := R;
    READ(INN,FF,C,D,E,F,G);
    ANN[QT+1+2*cnt].[7:8] := C;
    ANN[QT+1+2*cnt].[15:14] := D;
    ANN[QT+1+2*cnt].[19:18] := F;
    ANN[QT+1+2*cnt].[27:10] := E;
    ANN[QT+1+2*cnt].[37:11] := G;
  END;
  WRITE(PASSFILE[LINK1],30,ANN[*]);
  WRITE(SIMFILE,15,ANN[*]);
IF LINK NEQ 0 THEN
  BEGIN
    LINK1 := 1;
    GO TO RRD;
  END;
READ(INN,10,THING[*]);
END READEM;
%
%
%
PROCEDURE WRITEM;
BEGIN
  FORMAT F1("PTRBLK #",I4," IS ",A4,A3),
         F2(" PTR NO. ",I2," IT HAS ",I10," SEGS ",I10," FRAGS AND PTS TO PT
RBLK #",I4),
         F3("THE ABOVE LEVEL BLK PTS TO THE FOLLOWING//"),A4,A3,
         F4(" IT HAS ",I10," SEGS ",I10," FRAGS AND PTS TO PTRBLK#",I4),
         F5("PTRBLK #",I4," IS ",A4,A3),
         F6(" PTR NO. ",I2," IT HAS ",I10," SEGS ",I10," FRAGS, AND PTS TO PT
BLK #",I4),
         F7("THE ABOVE LEVEL BLK PTS TO THE FOLLOWING//"),
         F8("ASSNBLK #",I10,X5," PHASF =",I10," SEGS =",I10,X5,
"NEXT FRAG IN FILE IS AT ASSNBLK #",I10),
         F9("PHASED ASSNBLKS//"),
         F10("CONTIGUOUS ASSNBLKS//"),

```

```

F8(X12,"ASSNHLK #",I10,X5,"SEGS#",I10,X5,
"NEXT FRAG IN FILE IS AT ASNPLK #",I10),
F15(X50,"JUNK ASSNBLKS//"),
F16(X50,"THE FILE REQUEST WAS"),
F27("TOPBLK PTS TO//"),
FRT("FILE BLOCK #",I10," IS CALLED"),
FRT1("NO. OF SEGS/RCFD #",I10," TOTAL NO. OF SEGS #",I10,
" THE PREPROCESS REQUEST PTR IS ",I10),
FRT2(" THE POSTPROCESS PTR IS ",I10,
" THE FIRST FRAG IN THE FILE IS AT ASNPLK #",I10//),
FRT3(" IN TOPBLK, # OF SEGS #",I10," NO. OF FRAGS #",I10,
" HOLEGAN D001,RF,MI,D01,RE1,D02,DIDIT,D022,RF11,MI1),
ALPHA TYPE,WD3
ALPHA ARRAY ALA[0:9];
INTEGER ARRAY NXTEU[0:20],NXTSU[0:20],NXTTRK[0:20];
INTFGER EUNUMBFR,SIINUMBER,TRYNUMBER,VPP,SEGSS,FRAGSS,ANDY,
ANDYEU,CN3, ANDYSU,NM, PANDA,PHSS,NXTTT,CNT,A,RR,CD,E,ZZ,
CNT1,CNT2;
LAHFL ZZAZ,ZZAZ1,ZZAZ2,MAMA2,MAMA1,MAMA,LLVFLTR,LLVSUE,LLVTRKSU,
FINIT,HUBRA,CONF IN,HUBRA1,JNKFIN,HUBRA2,MURE1,BARA,HARA1,
HARA2,MAMAA,MAMAA1,MAMAA2;
D001=RE1=MI1=D0011=RF11=F022=RE111=MT11=FALSF;
FOR CNT:=0 STEP 1 UNTIL 9 DO REPLACF(ALA[CNT],0,THING[CNT],0,1);
FOR CNT := 0 STEP 1 UNTIL 2 DO
WRITF(SIMFILE,E,PTRPLK[0,3+CNT]);
WRITF(SIMFILE,F16);
WRITF(SIMFILE,F10,ALA[*]);
FOR CNT:=1 STEP 1 UNTIL NXFILE DO
BEGIN
REPLACE(ALA[0],0,AFILNAME(CNT),0,1);
REPLACE(ALA[1],0,BFILNAME(CNT),0,1);
REPLACE(ALA[2],0,CFILNAME(CNT),0,1);
A:= SEGSFECN(CNT);
B:= TOTSGFS(CNT);
C:= PEFTH(CNT);
[ := PUSTPTR(CNT); E:= FILASSN(CNT);
WRITF(SIMFILE,FPT,CNT);
WRITF(SIMFILE,3,ALA[*]);
WRITF(SIMFILE,FRT1,A,E); WRITE(SIMFILE,FRT2,D,F);
END;
NM := 1; A:= NUMSEGS(NM); B:= NUMFRAGS(NM);
WRITF(SIMFILE,FPT3,A,E);
CN3 := CNT1 := CNT2 := 0;
ANDY := PHYPTR(NM);
IF ANDY = 0 THEN GO TO LLVENTR;
WRITF(SIMFILE,F27);
ZZAZ:TYPE := "EU";
FNUMBER := NUMPFTR(ANDY);
VPF := VPPTTR(ANDY);
SEGSS := NUMSFGS(ANDY);
FRAGSS := NUMFRAGS(ANDY);
CN3 := CN3 + 1;
NXTFLU[CN3] := NXTPTR(ANDY);
ANDYEU := ANDY;
IF VPF=1 THEN WD:="PHYS" ELSE WD:="VIRT";
WRITF(SIMFILE,F,ANDY,WD,TYPE,EUNUMBER,SEGSS,FRAGSS,NXTFLU[CN3]);
ANDY := PHYPTR(ANDY);
IF ANDY < 0 THEN GO TO LLVSUF;
WRITF(SIMFILE,F?);
ZZAZ1:TYPE := "SU";
SNUMBER := NUMPFTR(ANDY);

```

```

VPP ← VPPTR(ANDY);
SEGSS ← NUMSEGS(ANDY);
FRAGSS ← NUMFRAGS(ANDY);
CNT1 := CNT1 + 1;
NXTSU[CNT1] ← NXTPTR(ANDY);
ANDYSU ← ANDY;
IF VPP=1 THEN WD1="PHYS" ELSE WD1="VIRT";
WRITE(SIMFILE,F3,ANDY,WD,TYPE,SEGSS,FRAGSS,NXTSU[CNT1]);
ANDY ← VPPTR(ANDY);
IF ANDY = 0 THEN GO TO LLVTRKSU;
WRITE(SIMFILE,F4);
ZZAZ2:TYPE ← "TRK";
TRKNUMBER ← NUMBPTR(ANDY);
VPP ← VPPTR(ANDY);
SEGSS ← NUMSEGS(ANDY);
FRAGSS ← NUMFRAGS(ANDY);
CNT2 := CNT2 + 1;
NXTTRK[CNT2] ← NXTPTR(ANDY);
IF VPP=1 THEN WD1="PHYS" ELSE WD1="VIRT";
WRITE(SIMFILE,F5,ANDY,WD,TYPE,TRKNUMBER,SEGSS,FRAGSS,
      NXTTRK[CNT2]);
ZZ := 3;
GO TO FINIT;
ILVELTB:
ANDY := NXTPTR(NM);
DO1 := TRUE;
IF ANDY ≠ 0 THEN BEGIN WRITE(SIMFILE,F27); GO TO ZZAZ3; END;
MAMA2:
ANDY := VSUPTR(NM);
FE ← TRUE;
IF ANDY ≠ 0 THEN BEGIN WRITE(SIMFILE,F27); GO TO ZZAZ1; END;
MAMA1:
ANLY := VTRKPTR(NM);
NI ← TRUE;
IF ANDY ≠ 0 THEN BEGIN WRITE(SIMFILE,F27); GO TO ZZAZ2; END;
MAMA2:ANDY := 1;
NI1 := TRUE;
ZZ := 0;
GO TO FINIT;
LLVSUEU:
ANDY ← VSUPTR(ANDYEU);
DO1 ← TRUE;
IF ANDY ≠ 0 THEN BEGIN WRITE(SIMFILE,F27); GO TO ZZAZ1; END;
MAMA3:
ANDY ← VTRKPTR(ANDYEU);
FE1 ← TRUE;
IF ANDY ≠ 0 THEN BEGIN WRITE(SIMFILE,F27); GO TO ZZAZ2; END;
MAMA3:ANDY := ANDYEU;
FF11 := TRUE;
ZZ := 1;
ANDYEU := 0;
GO TO FINIT;
LLVTRKSU:
ANDY ← VTRKPTR(ANDYSU);
DO2 ← TRUE;
IF ANDY ≠ 0 THEN BEGIN WRITE(SIMFILE,F4); GO TO ZZAZ2; END;
MAMA4:ZZ:=2;
DO22:=TRUE;
ANDY ← ANDYSU;
ANLYSU := 0;
FINIT:DIDIT := TRUE;

```

```

PANDA ← PHASPTR(ANDY);
CNT := 0;
HURBA1:
  IF PANDA = 0 THEN GO TO CONF1;
  PHSS ← PHNUM(PANDA);
  SEGSS ← SEGNUM(PANDA);
  NXTTT ← NXTFRAG(PANDA);
  IF DIDIT THEN BEGIN
    DIDIT := FALSE;
    CASE ZZ OF
      BEGIN
        WRITE(SIMFILE,F27);
        WRITE(SIMFILE,F2);
        WRITE(SIMFILE,F4);
        WRITE(SIMFILE,F6);
      END;
    END;
  IF CNT = 0 THEN
    WRITE(SIMFILE,F12);
    WRITE(SIMFILE,F8,PANDA,PHSS,SEGSS,NXTTT);
    PANDA ← NXTRL(PANDA);
    CNT := CNT + 1;
    GO TO HURBA1;
  CONF1:
    PANDA ← CONTIGPTR(ANDY);
    CNT := 0;
  HURBA1:
    IF PANDA = 0 THEN GO TO JNKFIN1;
    SEGSS ← SEGNUM(PANDA);
    NXTTT ← NXTFRAG(PANDA);
    IF DIDIT THEN
      BEGIN
        DIDIT := FALSE;
        CASE ZZ OF
          BEGIN
            WRITE(SIMFILE,F27);
            WRITE(SIMFILE,F2);
            WRITE(SIMFILE,F4);
            WRITE(SIMFILE,F6);
          END;
        END;
    IF CNT = 0 THEN
      WRITE(SIMFILE,F14);
      WRITE(SIMFILE,F8,PANDA,SEGSS,NXTTT);
      PANDA ← NXTRL(PANDA);
      CNT := CNT + 1;
      GO TO HURBA1;
  JNKFIN1:
    PANDA ← JUNKPTR(ANDY);
    CNT := 0;
  HURBA2:
    IF PANDA = 0 THEN GO TO MORF1;
    SEGSS ← SEGNUM(PANDA);
    NXTTT ← NXTFRAG(PANDA);
    IF DIDIT THEN
      BEGIN
        DIDIT := FALSE;
        CASE ZZ OF
          BEGIN
            WRITE(SIMFILE,F27);
            WRITE(SIMFILE,F2);
          END;
        END;
      END;
  
```

```

        WRITE(SIMFILE,F4);
        WRITE(SIMFILE,F6);
    END;
END;
IF CNT = 0 THEN
    WRITE(SIMFILE,F15);
    WRITE(SIMFILE,F8,PANDA,SFGSS,NXTTT);
    PANDA := NXTRLC(PANDA);
    CNT := CNT + 1;
    GO TO HUHBA2;
MORE1: IF CNT2 NEQ 0 THEN
    BEGIN
        ANDY := NXTRK(CNT2);
        CNT2 := CNT2 - 1;
        IF ANDY NEQ 0 THEN
            GO TO ZZAZZ ELSE GO TO MORE1;
    END;
    IF DO22 THEN GO TO BABAS;
    IF DO2 THEN IF ANDYSU NEQ 0 THEN GO TO MAMAA1 ELSE GO TO RARA;
    IF ANDYSU # 0 THEN GO TO LLVTRKSU;
RARA: IF RE11 THEN GO TO RABA1;
    IF DO2 THEN IF ANDYFU NEQ 0 THEN GO TO MAMAA ELSE GO TO RABA1;
    IF DO1 THEN IF ANDYEU NEQ 0 THEN GO TO MAMA ELSE GO TO RABA1;
    IF ANDYFU # 0 THEN GO TO LLVSUEU;
RARA1: IF CNT1 NEQ 0 THEN
    BEGIN
        ANDY := NXTSU(CNT1);
        CNT1 := CNT1 - 1;
        IF ANDY NEQ 0 THEN BEGIN
            DO2 := DO22 := FALSE;
            GO TO ZZAZ1; END ELSE GO TO RARA1;
        END;
        IF MI1 THEN GO TO RABA2;
        IF MI THEN GO TO MAMAA2;
        IF RE THEN GO TO MAMA1;
        IF DOU THEN GO TO MAMA2;
        GO TO LIVFUTR;
RARA2: IF CN3 NEQ 0 THEN
    BEGIN
        ANDY := NXTFU(CN3);
        CN3 := CN3 - 1;
        IF ANDY NEQ 0 THEN BEGIN
            DO2 := DO1 := RE1 := RF11 := DO22 := FALSE;
            GO TO ZZAZ;
        END ELSE GO TO RABA2;
    END;
    END;
    END;
    END;

```

D-3. SAMPLE OF EXECUTION OUTPUT

All of the output lines from the simulator itself are preceded by the word "SIM--". These lines contain the request number, queue information, time in a queue until allocation, simulated running time, processor time for procedures TREEBUILD and ALLOCATE, and the current system time.

0. **REQUEST 1** HAS JUST ENTERED QUEUE 8 AT SIMULATION TIME 0.
 THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 0.
 THE NUMBER OF REQUESTS IN QUEUE 0 IS 0.
 THE NUMBER OF REQUESTS IN QUEUE 1 IS 0.
 THE NUMBER OF REQUESTS IN QUEUE 2 IS 0.
 THE NUMBER OF REQUESTS IN QUEUE 3 IS 0.
 THE NUMBER OF REQUESTS IN QUEUE 4 IS 0.
 THE NUMBER OF REQUESTS IN QUEUE 5 IS 0.
 THE NUMBER OF REQUESTS IN QUEUE 6 IS 0.
 THE NUMBER OF REQUESTS IN QUEUE 7 IS 0.
 THE NUMBER OF REQUESTS IN QUEUE 8 IS 1.
 THE NUMBER OF REQUESTS IN QUEUE 9 IS 0.

IM-----QUEUEF	01-	TIME SHARD	IS	250 UNITS.	TIMESLICE	IS	250 UNITS.
IM-----QUEUEF	11-	TIME SHARD	IS	250 UNITS.	TIMESLICE	IS	250 UNITS.
IM-----QUEUEF	21-	TIME SHARD	IS	250 UNITS.	TIMESLICE	IS	250 UNITS.
IM-----QUEUEF	31-	TIME SHARD	IS	250 UNITS.	TIMESLICE	IS	250 UNITS.
IM-----QUEUEF	41-	TIME SHARD	IS	250 UNITS.	TIMESLICE	IS	250 UNITS.
IM-----QUEUEF	51-	TIME SHARD	IS	250 UNITS.	TIMESLICE	IS	250 UNITS.
IM-----QUEUEF	61-	TIME SHARD	IS	250 UNITS.	TIMESLICE	IS	250 UNITS.
IM-----QUEUEF	71-	TIME SHARD	IS	250 UNITS.	TIMESLICE	IS	250 UNITS.
IM-----QUEUEF	81-	TIME SHARD	IS	250 UNITS.	TIMESLICE	IS	250 UNITS.
IM-----QUEUEF	91-	TIME SHARD	IS	250 UNITS.	TIMESLICE	IS	250 UNITS.

18FL 100 OF SEGS/REQD = 8 TOTAL NO. OF SEGS = 7960 THE PREP/PROCESS REQUEST PTR IS
THE POSTPROCESS PTR IS C TMF FIRST FRG IN THE FILE IS AT ASSNRK 1
TITLE BLOCK # 1 IS CALIFO

218 CALIFORNIA

1 AFTI
NO. OF SEGSRECD = A TOTAL NO. OF SEGS = 7960 THE PREPROCESS REQUEST PTR IS 0
THE POSTPROCESS PTR IS 0 THE FIRST FRAG IN THE FILE IS AT ASSNBLK # 19

IN TOPBLK # OF SEGS = 14571, NO. OF FRAGS = 24
TOPBLK PTS TO

PTRBLK # 2 IS PHYS_EUPTR NO. 1 IT HAS 1201 SFGS 3 FRAGS AND PTS TO PTRBLK # 6
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 3 IS PHYS_SUPTR NO. 0 IT HAS 1200 SEGS 2 FRAGS AND PTS TO PTRBLK # 6
THE ABOVE LFVL BLK PTS TO THE FOLLOWING

PTRBLK # 4 IS PHYSTRKPTR NO. 0 IT HAS 1200 SFGS, 2 FRAGS, AND PTS TO PTRBLK # 0
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PHASED ASSNBLKS

ASSNBLK #	19	PHASE =	0 SFGS =	600 NAT FRAG IN FILE IS AT ASSNBLK # 26
ASSNBLK #	1	PHASE =	0 SEGS =	600 NAT FRAG IN FILE IS AT ASSNBLK # 2
PTRBLK #	8 IS PHYS_SUPTR NO. 1 IT HAS 1 SEGS	1 FRAGS AND PTS TO PTRBLK # 0	1 SFGS	1 FRAGS, AND PTS TO PTRBLK # 0

THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 9 IS PHYSTRKPTR NO. 1 IT HAS 1 SFGS, 1 FRAGS, AND PTS TO PTRBLK # 0
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

CONTIGUOUS ASSNBLKS

TOPBLK PTS TO ASSNBLK # 13 SEGS= 1 NXT FRAG IN FILE IS AT ASSNBLK # 14

PTRBLK # 10 IS VIRT_EUPTR NO. 1 IT HAS 2 SFGS 1 FRAGS AND PTS TO PTRBLK # 0
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 11 IS VIRT_SUPTR NO. 1 IT HAS 2 SEGS 1 FRAGS AND PTS TO PTRBLK # 0
THE ABOVE LFVL BLK PTS TO THE FOLLOWING

PTRBLK # 12 IS VIRTTRKPTR NO. 1 IT HAS 2 SFGS, 1 FRAGS, AND PTS TO PTRBLK # 0
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

JUNK ASSNBLKS

TOPBLK PTS TO ASSNBLK # 14 SEGS= 2 NXT FRAG IN FILE IS AT ASSNBLK # 15

PTRBLK # 5 IS VIRT_SUFTR NO. 1 IT HAS 483 SFGS 5 FRAGS AND PTS TO PTRBLK # 13

THE ABOVE LEVEL BLK PTS TO THF FOLLOWING

PHASED ASSNPLKS

ASSNBLK #	21	PHASE #	200 SEGS =	160	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNBLK #	3	PHASE #	300 SEGS =	160	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNBLK #	20	PHASE #	0 SEGS =	80	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNBLK #	2	PHASE #	0 SEGS =	80	NXT FRAG IN FILE IS AT ASSNBLK #
PTRBLK #	13 IS VIRT SUPTR NO. 2 IT HAS THE ABOVE LEVEL BLK PTS TO THF FOLLOWING	PTRBLK #	100 SEGS =	3	NXT FRAG IN FILE IS AT ASSNBLK #
			4 SEGS =	1	FRAGS AND PTS TO PTRBLK #

CONTIGUOUS ASSNBLKS

TOPBLK PTS TO ASSNBLK # 16 SEGS= 4 NXT FRAG IN FILE IS AT ASSNBLK # 17

PTRBLK # 14 IS VIRTTRKPTR NO. 2 IT HAS
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PHASED ASSNPLKS

ASSNPLK #	17	PHASE #	200 SEGS =	6	NXT FRAG IN FILE IS AT ASSNBLK #
PTRBLK #	15 IS VIRTTRKPTR NO. 1 IT HAS THE ABOVE LEVEL BLK PTS TO THE FOLLOWING		0 SFGS,	1	FRAGS, AND PTS TO PTRBLK # 0

JUNK ASSNPLKS

TOPBLK PTS TO ASSNPLK # 18 SEGS= 6 NXT FRAG IN FILE IS AT ASSNBLK # 0

CONTIGUOUS ASSNBLKS

ASSNPLK #	24	SEGS=	1600	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNPLK #	6	SEGS=	1600	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNPLK #	22	SEGS=	800	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNPLK #	4	SEGS=	400	NXT FRAG IN FILE IS AT ASSNBLK #

ASSNBLK #	23	SEGS=	4000	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNBLK #	5	SEGS=	4000	NXT FRAG IN FILE IS AT ASSNBLK #
PTRBLK #	6 IS PHYS EUPTR NO. 2 IT HAS THE ABOVE LEVEL BLK PTS TO THE FOLLOWING		19 SFGS	2 FRAGS AND PTS TO PTRBLK # 7

PHASED ASSNPLKS

ASSNBLK # 7 PHASE # 300 SFGS = 9 NXT FRAG IN FILE IS AT ASSNBLK # 0

ASSNBLK # 7 IS PHYS EUPTR NO. 4 IT HAS
PTRLK # 7 IS PHYS EUPTR NO. 4 IT HAS
THE APROV LVEL RLK PTS TO THE FOLLOWING

10 NXT FRAG IN FILE IS AT ASSNBLK # 9
08 SFGS 4 FRAGS AND PTS TO PT RBLK # 0

CONTIGUOUS ASSNBLKS

ASSNBLK #	12	SEGS#	12	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNBLK #	11	SEGS#	12	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNBLK #	10	SFGS#	12	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNBLK #	9	SEGS#	12	NXT FRAG IN FILE IS AT ASSNBLK #

SIM--REQUEST 1 WAS JUST ALLOCATED AFTFR WAITING 20 UNITS OF SIMULATION TIME IN QUEUE 6
 SIM--SIMTIME NOW IS 28.
 SIM--REQUEST 1 -PROCESSOR TIME FOR ALLOCATION IS 226.
 SIM--THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 1.
 SIM--THE NUMBER OF REQUESTS IN QUEFL 01 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEFL 11 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEFL 21 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEFL 31 IS 0.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 41 IS 0.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 51 IS 0.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 61 IS 0.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 71 IS 0.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 81 IS 1.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 91 IS 0.*

SIM--REQUEST 3 HAS JUST ENTERED QUEFL 9 AT SIMULATION TIME 67.
 SIM--THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 1.
 SIM--THE NUMBER OF REQUESTS IN QUEFL 01 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEFL 11 IS 0.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 21 IS 0.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 31 IS 0.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 41 IS 0.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 51 IS 0.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 61 IS 0.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 71 IS 0.*
 SIM--THE NUMBER OF REQUESTS IN QUEFL 81 IS 1.*
 SIM--ALLOCATION ATTEMPT TO PE MADE ON QUEFL 81.
 SIM--REQUEST 2 - PROCESSOR TIME FOR TREERBLD IS 324.

000Y, OH
 0\$02050>
 00006006

(0E01@SU01@THK01@01600 SEGMENTS)),SU11@10,010,010,M\$170),100C,500,200C)
 FILE BLOCK # 1 IS CALFD
 16FL
 NO. OF SEGS/SEGCD = 0 TOTAL NO. OF SEGGS = 7960 THE PREPROCESS REQUEST PTR IS
 THE POSTPROCESS PTR IS 0 THE FIRST FRAG IN THE FILE IS AT ASSNBLK # 0

FILE BLOCK # 2 IS CALLED

IAFIL

NO. OF SEGS/RECD = 15 0 TOTAL NO. OF SEGS = 7960 THE PREP-PROCESS REQUEST PTR IS 0
THE POSTPROCESS PTR IS 0 THE FIRST FRAG IN THE FILE IS AT ASSNBLK # 19

IN TOPBLK, # OF SEGS = 10571, NO. OF FRAGS = 24
TOPBLK PTS TO

PTRBLK # 2 IS PHYS EUPTR NO. 1 IT HAS 1201 SEGS 3 FRAGS AND PTS TO PT RBLK # 6
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 3 IS PHYS SUPT NO. 0 IT HAS 1200 SEGS 2 FRAGS AND PTS TO PTRBLK
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 4 IS PHYSRKPTR NO. 0 IT HAS 1200 SEGS, 2 FRAGS, AND PTS TO PTR BLK # 0
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PHASED ASSNPLKS

ASSNBLK #	19	PHASE #	0 SEGS = 600	NXT FRAG IN FILE IS AT ASSNBLK # 20
ASSNBLK #	1	PHASE #	0 SEGS = 600	NXT FRAG IN FILE IS AT ASSNBLK # 2
PTRBLK #	6 IS PHYS SUPT NO. 1 IT HAS 1 SEGS		1 FRAGS AND PTS TO PTRBLK 0	

THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 9 IS PHYSRKPTR NO. 1 IT HAS 1 SEGS, 1 FRAGS, AND PTS TO PTR BLK # 0
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

CONTIGUOUS ASSNBLK

TOPBLK PTS TO ASSNBLK # 13 SEGS = 1 NXT FRAG IN FILE IS AT ASSNBLK # 14

PTRBLK # 10 IS VIRT EUPTR NO. 1 IT HAS 2 SEGS 1 FRAGS AND PTS TO PT RBLK # 0
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 11 IS VIRT RKPTR NO. 1 IT HAS 2 SEGS 1 FRAGS AND PTS TO PTRBLK 0
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 12 IS VIRT RKPTR NO. 1 IT HAS 2 SEGS, 1 FRAGS, AND PTS TO PTR BLK # 0
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

JUNK ASSNPLKS

TOPBLK PTS TO ASSNBLK # 14 SEGS = 2 NXT FRAG IN FILE IS AT ASSNBLK # 15

PTBLK # 5 IS VIRT SUPTR NO. 1 IT HAS
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

4A3 SFGS 5 FRAGS AND PTS TO PTBLK 13

PHASED ASSNPLKS

ASSNBLK #	21	PHASE =	300	SEGS =	160	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNBLK #	3	PHASE =	300	SEGS =	160	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNBLK #	20	PHASE =	0	SEGS =	80	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNBLK #	2	PHASE =	0	SEGS =	80	NXT FRAG IN FILE IS AT ASSNBLK #
ASSNBLK #	15	PHASE =	100	SEGS =	3	NXT FRAG IN FILE IS AT ASSNBLK #
PTBLK #	13 IS VIRT SUPTR NO. 2 IT HAS THE ABOVE LEVEL BLK PTS TO THE FOLLOWING		4 SFGS	I FRAGS AND PTS TO PTBLK 0		

CONTIGUOUS ASSNPLKS

TOPBLK PTS TO ASSNBLK # 16 SFGS= 4 NXT FRAG IN FILE IS AT ASNBLK # 17

PTBLK # 14 IS VIRT SUPTR NO. 2 IT HAS
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PHASED ASSNPLKS

ASSNBLK #	17	PHASE =	200	SEGS =	6	NXT FRAG IN FILE IS AT ASSNBLK #
PTBLK #	15 IS VIRT SUPTR NO. 1 IT HAS THE ABOVE LEVEL BLK PTS TO THE FOLLOWING		8 SFGS,	I FRAGS, AND PTS TO PTBLK 0		

JUNK ASSNPLKS

TOPBLK PTS TO ASSNBLK # 18 SFGS= 8 NXT FRAG IN FILE IS AT ASNBLK # 6

CONTIGUOUS ASSNPLKS

ASSNBLK #	24	SEGS=	1600	NXT FRAG IN FILE IS AT ASNBLK #
ASSNBLK #	6	SEGS=	1600	NXT FRAG IN FILE IS AT ASNBLK #
ASSNBLK #	22	SEGS=	800	NXT FRAG IN FILE IS AT ASNBLK #
ASSNBLK #	4	SEGS=	800	NXT FRAG IN FILE IS AT ASNBLK #
			JUNK ASSNBLKS	

ASSNBLK #	23	SEGS=	4000	NXT FRAG IN FILE IS AT ASNBLK #
ASSNBLK #	5	SEGS=	4000	NXT FRAG IN FILE IS AT ASNBLK #
PTBLK #	6 IS PHYS SUPTR NO. 2 IT HAS THE ABOVE LEVEL BLK PTS TO THE FOLLOWING		19 SFGS	2 FRAGS AND PTS TO PTBLK 7

PHASED ASSNPLKS

ASSNBLK # 7 PHASE = 300 SEGS = 9 NXT FRAG IN FILE IS AT ASSNBLK # 6
JUNK ASSNRLs

ASSNBLK # 7 IS PHYS EUPTR NO. 8 SEGS =
PTRBLK # THE ABOVE LEVEL RLK PTS TO THE FOLLOWING
4 IT HAS
46 SFGS

10 NXT FRAG IN FILE IS AT ASSNBLK # 5
4 SFGS AND PTS TO PT RLK # 0

CONTIGUOUS ASSNBLKS

ASSNBLK #	12	SEGS#	12	NXT FRAG IN FILE IS AT ASSNBLK # 13
ASSNBLK #	11	SEGS#	12	NXT FRAG IN FILE IS AT ASSNBLK # 12
ASSNBLK #	10	SEGS#	12	NXT FRAG IN FILE IS AT ASSNBLK # 11
ASSNBLK #	9	SEGS#	12	NXT FRAG IN FILE IS AT ASSNBLK # 10

SIM==REQUEST 2 WAS JUST ALLOCATED AFTER WAITING 39 UNITS OF SIMULATION TIME IN QUEUE 6

SIM==REQUEST 2 =PROCESSOR TIME FOR ALLOCATION IS 225.
SIM==THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 2.
SIM==THE NUMBER OF REQUESTS IN QUFUL 0 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 1 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 2 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 3 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 4 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 5 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 6 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 7 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 8 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 9 IS 1.

SIM==REQUEST 4 HAS JUST ENTERED QUFUL 1 AT SIMULATION TIME 145.
SIM==THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 2.
SIM==THE NUMBER OF REQUESTS IN QUFUL 0 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 1 IS 1.
SIM==THE NUMBER OF REQUESTS IN QUFUL 2 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 3 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 4 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 5 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 6 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 7 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 8 IS 0.
SIM==THE NUMBER OF REQUESTS IN QUFUL 9 IS 1.
SIM==ALLOCATION ATTEMPT TO RE MADE ON QUFUL 1.
SIM==REQUEST 4 = PROCESSOR TIME FOR TREBUILD IS 329.

000Y, 0H
00020502
00006006

THE FILE REQUEST WAS
(EUF1\PSUD\ETRKO\01600 SEGMENTS)),SU1(\#010,\#10 MS120),100C,500,200C)
FILE BLOCK # 1 IS CALLED

18FIL NO. OF SEGS/RECD = 0 TOTAL NO. OF SEGS = 7960 THE PREPROCESS REQUEST PTR IS 0
 THE POSTPROCESS PTR IS 0 THE FIRST FRAG IN THE FILE IS AT ASSNBLK # 0

FILE BLOCK # 2 IS CALLED

1A1L NO. OF SEGS/RECD = 0 TOTAL NO. OF SEGS = 7960 THE PREPROCESS REQUEST PTR IS 0
 THE POSTPROCESS PTR IS 0 THE FIRST FRAG IN THE FILE IS AT ASSNBLK # 19

IN TOPBLK, # OF SEGS = 14571, NO. OF FRAGS = 24

TOPBLK PTS TO

PTRBLK # 2 IS PHYS EUPTR NO. 1 IT HAS 1201 SFGS 3 FRAGS AND PTS TO PT RBLK # 6
 THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 3 IS PHYS SUPTR NO. 0 IT HAS 1200 SFGS 2 FRAGS AND PTS TO PTRBLK 0
 THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 4 IS PHYSTRKPT NO. 0 IT HAS 1200 SFGS, 2 FRAGS, AND PTS TO PTR BLK # 0
 THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PHASED ASSNBLKS

ASSNBLK # 19	PHASE = 0	SEGS = 600	NXT FRAG IN FILE IS AT ASSNBLK # 20
ASSNBLK # 1	PHASE = 0	SEGS = 600	NXT FRAG IN FILE IS AT ASSNBLK # 2
PTRBLK # 8 IS PHYS SUPTR NO. 1 IT HAS 1 SEG#		1	FRAGS AND PTS TO PTRBLK 0

THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 9 IS PHYSTRKPT NO. 1 IT HAS 1 SFGS, 1 FRAGS, AND PTS TO PTR BLK # 0
 THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

CONTIGUOUS ASSNBLKS

TOPBLK PTS TO ASSNBLK # 13 SEGS# 1 NXT FRAG IN FILE IS AT ASSNBLK # 14

PTRBLK # 10 IS VIRT EUPTR NO. 1 IT HAS 2 SEG# 1 FRAGS AND PTS TO PT RBLK # 0
 THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 11 IS VIRT SUPTR NO. 1 IT HAS 2 SEG# 1 FRAGS AND PTS TO PTRBLK 0
 THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 12 IS VIRTTRKPT NO. 1 IT HAS 2 SFGS, 1 FRAGS, AND PTS TO PTR BLK # 0
 THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

JUNK ASSNBLKS

TOPBLK PTS TO ASSNBLK # 14 SEGSS#

2 NXT FRAG IN FILE IS AT ASNBLK # 15

PTRBLK # 5 IS VIRT SUPTR NO. 1 IT HAS
THE ABOVE LEVEL BLK PTS TO THF FOLLOWING

4&3 SEGSS 5 FRAGS AND PTS TO PTRBLK 13

PHASED ASSNBLKS

ASSNBLK #	21	PHASE #	300 SEGSS #	160	NXT FRAG IN FILE IS AT ASNBLK #
ASSNBLK #	3	PHASE #	300 SEGSS #	160	NXT FRAG IN FILE IS AT ASNBLK #
ASSNBLK #	20	PHASE #	0 SEGSS #	80	NXT FRAG IN FILE IS AT ASNBLK #
ASSNBLK #	2	PHASE #	0 SEGSS #	80	NXT FRAG IN FILE IS AT ASNBLK #
ASSNBLK #	15	PHASE #	100 SEGSS #	3	NXT FRAG IN FILE IS AT ASNBLK #
PTRBLK # 13 IS VIRT SUPTR NO. 2 IT HAS THE ABOVE LEVEL BLK PTS TO THF FOLLOWING		4 SEGSS	1 ERAGS AND PTS TO PTRBLK 0		

CONTIGUOUS ASSNBLKS

TOPBLK PTS TO ASSNBLK # 16 SEGSS#

4 NXT FRAG IN FILE IS AT ASNBLK # 17

PTRBLK # 14 IS VIRTTRKPTR NO. 2 IT HAS
THE ABOVE LEVEL BLK PTS TO THF FOLLOWING

6 SEGSS, 1 FRAGS, AND PTS TO PTR BLK # 15

PHASED ASSNBLKS

ASSNBLK #	17	PHASE #	200 SEGSS #	6	NXT FRAG IN FILE IS AT ASNBLK #
PTRBLK # 15 IS VIRTTRKPTR NO. 1 IT HAS THE ABOVE LEVEL BLK PTS TO THF FOLLOWING		6 SEGSS,	1 FRAGS, AND PTS TO PTR BLK # 0		

JUNK ASSNBLKS

TOPBLK PTS TO ASSNBLK # 18 SEGSS#

8 NXT FRAG IN FILE IS AT ASNBLK # 0

CONTIGUOUS ASSNBLKS

ASSNBLK #	24	SEGSS#	1600	NXT FRAG IN FILE IS AT ASNBLK #
ASSNBLK #	6	SEGSS#	1600	NXT FRAG IN FILE IS AT ASNBLK #
ASSNBLK #	22	SEGSS#	800	NXT FRAG IN FILE IS AT ASNBLK #
ASSNBLK #	4	SEGSS#	800	NXT FRAG IN FILE IS AT ASNBLK #
			JUNK ASSNBLKS	

ASSNBLK #	23	SEGSS#	4000	NXT FRAG IN FILE IS AT ASNBLK #
ASSNBLK #	5	SEGSS#	4000	NXT FRAG IN FILE IS AT ASNBLK #
PTRBLK # 6 IS PHYS SUPTR NO. 2 IT HAS THE ABOVE LEVEL BLK PTS TO THF FOLLOWING		19 SEGSS	2 FRAGS AND PTS TO PTR BLK # 7	

PHASED ASSNBLKS

ASSNBLK #	7	PHASF =	300 SFCS =	9	NXT FRAG IN EIL IS AT ASSNBLK #	6
JUNK ASSNBLKS						

ASSNBLK # 6 SEGS#
PTBLK # 7 IS PHYS EUPTR NO. & IT HAS
THE ABOVE LEVEL ALK PTS TO THE FOLLOWING

10 SFCS NXT FRAG IN FILE IS AT ASSNBLK # 9
4 SFCS & ERAGS AND PTS TO PT RBLK # 0

CONTIGUOUS ASSNBLKS

ASSNBLK #	12	SEGS#	12	NXT FRAG IN EIL IS AT ASSNBLK #	13
ASSNBLK #	11	SEGS#	12	NXT FRAG IN FILE IS AT ASSNBLK #	12
ASSNBLK #	10	SEGS#	12	NXT FRAG IN FILE IS AT ASSNBLK #	11
ASSNBLK #	9	SEGS#	12	NXT FRAG IN FILE IS AT ASSNBLK #	10

SIM--REQUEST 4 WAS JUST ALLOCATED AFTER WAITING 0 UNITS OF SIMULATION TIME IN QUEUE 1
 SIM--SIMTIME NOW IS 145.
 SIM--REQUEST 4 =PROCESSOR TIME FOR ALLOCATION IS 155.
 SIM--THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 3.
 SIM--THE NUMBER OF REQUESTS IN QUEUFL 0 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEUF 1 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEUF 2 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEUF 3 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEUF 4 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEUF 5 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEUF 6 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEUF 7 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEUF 8 IS 0.
 SIM--THE NUMBER OF REQUESTS IN QUEUF 9 IS 1.

SIM--REQUEST 1 IS FINISHED AFTER 123 UNITS OF TIME.

SIM--QUEUEU 01- TIMESHARD IS 250 UNITS. TIMESLICE IS 250 UNITS.
 SIM--QUEUEU 11- TIMESHARD IS 250 UNITS. TIMESLICE IS 250 UNITS.
 SIM--QUEUEU 21- TIMESHARD IS 250 UNITS. TIMESLICE IS 250 UNITS.
 SIM--QUEUEU 31- TIMESHARD IS 250 UNITS. TIMESLICE IS 250 UNITS.
 SIM--QUEUEU 41- TIMESHARD IS 250 UNITS. TIMESLICE IS 250 UNITS.
 SIM--QUEUEU 51- TIMESHARD IS 250 UNITS. TIMESLICE IS 250 UNITS.
 SIM--QUEUEU 61- TIMESHARD IS 250 UNITS. TIMESLICE IS 250 UNITS.
 SIM--QUEUEU 71- TIMESHARD IS 250 UNITS. TIMESLICE IS 250 UNITS.
 SIM--QUEUEU 81- TIMESHARD IS 250 UNITS. TIMESLICE IS 127 UNITS.
 SIM--QUEUEU 91- TIMESHARD IS 250 UNITS. TIMESLICE IS 250 UNITS.
 SIM--ALLOCATION ATTEMPT TO RE MAOF ON QUEUFL 9].
 SIM--REQUEST 3 = PROCESSOR TIME FOR TREERUILD IS 322.

000Y, OH
0002050>
00006006

(@E01C@S00C@TRK0C@01600 SEGMENTS)), SH1[PCT10, P10 MS:20], FILE REQUEST PTR IS
 FILE BLOCK # 1 IS CALLED
 IBFIL
 NO. OF SEGS/RECD = 8 TOTAL NO. OF SEGS = 7960 THF PREPROCESS REQUEST PTR IS 0
 THE POSTPROCESS PTR IS 0 THE FIRST FRAG IN THE FILE IS AT ASSMBLK # 0

FILE BLOCK # 2 IS CALLED
 IAFIL
 NO. OF SEGS/RECD = 8 TOTAL NO. OF SEGS = 7960 THF PREPROCESS REQUEST PTR IS 0
 THE POSTPROCESS PTR IS 0 THE FIRST FRAG IN THE FILE IS AT ASSMBLK # 19

IN TOPBLK, # OF SEGS = 14571, NO. OF FRAGS = 24

PTRBLK # 2 IS PHYS EUPTR NO. 1 IT WAS 1201 SFGS 3 FRAGS AND PTS TO PT RBLK # 6
 THE ABOVE LEVEL BLK PTS TO THF FOLLOWING

PTRBLK # 3 IS PHYS SUPTR NO. 0 IT HAS 1200 SFGS 2 FRAGS AND PTS TO PTRBLK # 6
 THE ABOVE LEVEL BLK PTS TO THF FOLLOWING

PTRBLK # 4 IS PHYSTRKPTR NO. 0 IT HAS 1200 SFGS, 2 FRAGS, AND PTS TO PTR BLK # 0
 THE ABOVE LFVEL BLK PTS TO THF FOLLOWING

PHASED ASSMBLK'S

ASSMBLK # 19	PHASE # 0	SEGS # 600	NXT FRAG IN FILE IS AT ASSMBLK # 20
ASSMBLK # 1	PHASE # 0	SEGS # 600	NXT FRAG IN FILE IS AT ASSMBLK # 2
PTRBLK # 6 IS PHYS SUPTR NO. 1 IT HAS 1 SFGS, 1 FRAGS, AND PTS TO PTRBLK # 0 THE ABOVE LFVEL BLK PTS TO THE FOLLOWING		1 SEGS	

PTRBLK # 9 IS PHYSTRKPTR NO. 1 IT HAS 1 SFGS, 1 FRAGS, AND PTS TO PTR BLK # 0
 THE ABOVE LFVEL BLK PTS TO THF FOLLOWING

CONTIGUOUS ASSMBLK'S

TOPBLK PTS TO ASSMBLK # 13 SFGS = 1	NXT FRAG IN FILE IS AT ASSMBLK # 14
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PTRBLK # 10 IS VIRT EUPTR NO. 1 IT HAS 2 SEGS 1 FRAGS AND PTS TO PT RBLK # 0
 THE ABOVE LEVEL BLK PTS TO THE FOLLOWING

PTRBLK # 11 IS VIRT SUPTR NO. 1 IT HAS 2 SEGS 1 FRAGS AND PTS TO PTRBLK # 0
 THE ABOVE LEVEL BLK PTS TO THF FOLLOWING

PTRBLK # 12 IS VIRTTRKPTR NO. 1 IT HAS 2 SFGS, 1 FRAGS, AND PTS TO PTR BLK # 0
 THE ABOVE LEVEL BLK PTS TO THF FOLLOWING

JUNK ASSNBLKS

TOPBLK PTS TO ASSNBLK # 14 SEG# 2 NXT FRAG IN FILE IS AT ASNBLK # 15

PTBLK # 5 IS VIRT SUPTR NO. 1 IT HAS
THE ABOVE LFUEL BLK PTS TO THE FOLLOWING

PTBLK # 5 FRAGS AND PTS TO PTBLK # 13

PHASED ASSNBLKS

ASSNBLK #	21	PHASE #	300	SFGS #	160	NXT FRAG IN FILE IS AT ASNBLK #	22
ASSNBLK #	3	PHASE #	300	SFGS #	160	NXT FRAG IN FILE IS AT ASNBLK #	4
ASSNBLK #	20	PHASE #	0	SFGS #	60	NXT FRAG IN FILE IS AT ASNBLK #	21
ASSNBLK #	2	PHASE #	0	SFGS #	60	NXT FRAG IN FILE IS AT ASNBLK #	3
ASSNBLK #	15	PHASE #	100	SFGS #	3	NXT FRAG IN FILE IS AT ASNBLK #	16
PTBLK # 13 IS VIRT SUPTR NO. 2 IT HAS			4	SFGS #	1	FRAGS AND PTS TO PTBLK # 0	
THE ABOVE LEVEL BLK PTS TO THE FOLLOWING							

CONTIGUOUS ASSNBLKS

TOPBLK PTS TO ASSNBLK # 16 SEG# 4 NXT FRAG IN FILE IS AT ASNBLK # 17

PTBLK # 14 IS VIRTTRPTR NO. 2 IT HAS
THE ABOVE LFUEL BLK PTS TO THE FOLLOWING

PHASED ASSNBLKS

ASSNBLK #	17	PHASE #	200	SFGS #	6	NXT FRAG IN FILE IS AT ASNBLK #	16
PTBLK #	15 IS VIRTTRPTR NO. 1 IT HAS		8	SFGS #	1	FRAGS AND PTS TO P TR BLK # 0	
THE ABOVE LFUEL BLK PTS TO THE FOLLOWING							

JUNK ASSNBLKS

TOPBLK PTS TO ASSNBLK # 18 SEG# 6 NXT FRAG IN FILE IS AT ASNBLK # 0

CONTIGUOUS ASSNBLKS

ASSNBLK #	24	SEG#	1600	NXT FRAG IN FILE IS AT ASNBLK #	1
ASSNBLK #	6	SEG#	1600	NXT FRAG IN FILE IS AT ASNBLK #	7
ASSNBLK #	22	SEG#	600	NXT FRAG IN FILE IS AT ASNBLK #	23
ASSNBLK #	4	SEG#	600	NXT FRAG IN FILE IS AT ASNBLK #	5
JUNK ASSNBLKS					

ASSNBLK # 23 SEG# 4000 NXT FRAG IN FILE IS AT ASNBLK # 24

PTRBLK # 5 ASSMBLK # 6 IS PHYS EUPTR NO. 5 SFGS= 4000 SFCS NEXT FPAG IN FILE IS AT ASNBLK # 7
THF ADOVF LEVEL BLK PTS TO THF FOLLOWING

PTRBLK # 7 IS PHYS EUPTR NO. 4 IT HAS 4000 SFCS NEXT FPAG IN FILE IS AT ASNBLK # 6
THF ABOVE LFLVL BLK PTS TO THE ENDING

PHASSED ASSNBLKS

ASSMBLK #	7	PHASE =
ASSMBLK #	7	300 SFGS = JUNK ASNBLKS

ASSMBLK # 6 IS PHYS EUPTR NO. 6 SFGS= 10 NEXT FRAG IN FILE IS AT ASNBLK # 9
THF ABOVE LFLVL BLK PTS TO THE ENDING

CONTIGUOUS ASNBLKS

ASSMBLK #	12	SEGS=	12	NEXT FPAG IN FILE IS AT ASNBLK # 13
ASSMBLK #	11	SFGS=	12	NEXT FPAG IN FILE IS AT ASNBLK # 12
ASSMBLK #	10	SFGS=	12	NEXT FRAG IN FILE IS AT ASNBLK # 11
ASSMBLK #	9	SFGS=	12	NEXT FRAG IN FILE IS AT ASNBLK # 10

SIM==REQUEST 3 WAS JUST ALLOCATED AFTER WAITING 64 UNITS OF SIMULATION TIME IN QUEUE 9

SIM==SIMTIME NOW IS 151.

SIM==REQUEST 3 =PROCESSOR TIME FOR ALLOCATION IS 65.

SIM==THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 3.

SIM==THE NUMBER OF REQUESTS IN QUFUL 0 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 1 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 2 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 3 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 4 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 5 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 6 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 7 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 8 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 9 IS 0.

SIM==REQUEST 5 HAS JUST ENTERED QUFUL 1 AT SIMULATION TIME 174.
SIM==THE NUMBER OF REQUESTS ALREADY ALLOCATED IS 3.

SIM==THE NUMBER OF REQUESTS IN QUFUL 0 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 1 IS 1.

SIM==THE NUMBER OF REQUESTS IN QUFUL 2 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 3 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 4 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 5 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 6 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 7 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 8 IS 0.

SIM==THE NUMBER OF REQUESTS IN QUFUL 9 IS 0.

SIM==ALLOCATION ATTEMPT TO RE MAPD ON QUEUE[1].

***** -OPRTR DS=ED SIRPLA / TANISK = 1, S = 110, A = 10 *****

LIST OF REFERENCES

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- [5] Parnas, David L. and Darringer, John A., "SODAS and a Methodology for System Design," Proc. Fall Joint Computer Conference (1967) pp. 449-474.
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UNCLASSIFIED

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ABSTRACT <p>This report gives a discussion of the field of simulation. The use of the simulation language SIMULA is then used to program general disk storage allocation simulators with application for use in testing allocation algorithms for the ILLIAC IV disk file allocator. Finally the concept of system design by using simulation in the design phase at various design levels is presented, with emphasis on using SIMULA for design from the hardware level upward.</p>		

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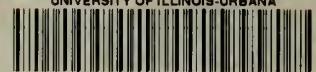
14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
ILLIAC IV						
SIMULA						
Simulation						
Storage allocation						
Disk file allocation						
Systems design						

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